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# Flexible small-channel thin-film transistors by electrohydrodynamic lithography†

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Small-channel organic thin-film transistors (OTFTs) are an essential component of microelectronic devices. With the advent of flexible electronics, the fabrication of OTFTs still faces numerous hurdles in the realization of highly-functional, devices of commercial value. Herein, a concise and efficient procedure is proposed for the fabrication of flexible, small-channel organic thin-film transistor (OTFT) arrays on large-area substrates that circumvents the use of photolithography. By employing a low-cost and high-resolution mechano-electrospinning technology, large-scale micro/nanofiber-based patterns can be digitally printed on flexible substrates (Si wafer or plastic), which can act as the channel mask of TFT instead of a photolithography reticle. The dimensions of the micro/nanochannel can be manipulated by tuning the processing parameters such as the nozzle-to-substrate distance, applied voltage, and fluid supply. The devices exhibit excellent electrical properties with high mobilities (~0.62 $cm^2 V^{-1} s^{-1}$) and high on/off current ratios (~$2.47 \times 10^6$), and they are able to maintain stability upon being bent from 25 mm to 2.75 mm (bending radius) over 120 testing cycles. This electrohydrodynamic lithography-based approach is a digital, programmable, and reliable alternative for easily fabricating flexible, small-channel OTFTs, which can be integrated into flexible and wearable devices.

## Introduction

Organic thin-film transistors hold much potential for realizing low-cost, industrial-grade microelectronic devices, which can be fabricated using facile approaches.[1–8] Considerable effort has gone into developing more effective organic semiconductor materials[9–11] and improving the fabrication procedure of the OTFTs[12–16] in order to realize this potential. The 'feature size' of a transistor is the length of the channel between the source electrodes and drain electrodes, and the fabrication of the channel (typically a micro/nanochannel) is a critical process in the construction of large-area transistor arrays. Although many fabrication procedures employ top-down methods,[17–20] two common approaches involve the etching of nanoscale trenches into the silicon or glass substrate, using high-resolution lithography (such as electron beam,[17] focused ion beam,[18] laser,[19] *etc.*) and the use of a template (molding).[21] Sacrificial techniques for fabricating nanostructures have also been employed, in which an e-beam or high-resolution photolithography is used to pattern a sacrificial material coated as a deposited film, followed by a wet etch of the sacrificial material. However, these approaches are expensive and require elaborate procedures, which in turn make it very challenging to obtain narrow channels, particularly on large-area flexible substrates. This drawback applies to all new strategies that use nanorod[12,22] as the template of nanochannel and so on.[23,24]

A digital mask or mask-free process on a large scale tends to be a data-driven and easy to modify method, making it possible to customize requirements and showing great promise in the rapid development of micro/nanodevices. This simplifies the process and saves material in the fabrication. Micro/nanochannels with the conducting polymer poly(3,4-ethylenedioxithiophene) doped with poly(styrene sulfonate) (PEDOT/PSS) and silver nanoparticles were fabricated.[25,26] Although a small-channel size could be obtained for "test devices", the same level of performance could not be realized for large-area devices. Inkjet printing[27] and electrohydrodynamic printing[28] have been used to fabricate the source and drain electrodes with a gap of 100 μm. These processes depend on the accuracy of the platform and it is not possible to achieve high-resolution manufacturing. Recently, MES has been found to be a

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low-cost, high efficiency, high-resolution printing technology and has shown great promise for the manufacture of high-resolution micro/nanofibers for uniform patterned masks.[29] Using this approach, the dimensions can be well controlled by adjusting parameters such as the applied voltage,[30] and micro/nanochannels can be formed using electrospun fibers instead of lithography resist patterns as etch masks.[31–35] Using this approach, Y. Ishii[32] and Sung-Yong Min[34] fabricated a bottom-gate, bottom-contact (BGBC) OTFT device by depositing a thin pentacene layer onto the gap electrodes. This route did not simplify the processes compared to those of conventional lithography, and the overall performance of the transistor diminished due to the higher contact resistance and the uneven interface between the semiconductor and the insulating layer, in comparison with a bottom-gate, top-contact structure (BGTC).

A programmable, photolithography-free and cost-effective procedure for the fabrication of high-performance OTFT device and large-area TFT arrays on ultrathin flexible substrates with the resolution being comparable with that of photolithography is proposed in this study. Based on MES direct-writing, micro/nanofibers with different dimensions can be obtained with programmable parameters, and the micro/nanochannels and OTFT can be fabricated followed by the fibers. The fibers can be designed to have the characteristics of a nearly circular cross section, thus acting as the mask during the thermal evaporation. Fig. 1a and the inset figure give a schematic of the structure of TFTs constructed using a continuous microfiber. The electrical capability and stability of the TFT device were tested under ambient conditions.

## Results and discussion

Fig. 1b shows the fabrication of transistors, which involves six steps: (1) preparing the gold and chromium bilayer (200 nm and 10 nm respectively) by thermal vacuum evaporation as the gate electrode and the aluminium oxide layer (20 nm) by Atomic Layer Deposition (ALD) as the insulation layer, on the flexible substrate under temperatures of 150–200 °C; (2) spin-coating the diketopyrrolopyrrole-based π-conjugated copolymer (PDPP5T) on $Si/SiO_2$ substrates and annealing for 10 minutes to form the semiconductor layer (50 nm); (3) spreading a layer of *n*-hexane on the substrate for collecting nano/microfibers; (4) direct-writing the polymer fibers *via* Mechano-electrospinning (MES)[36] as a fine mask of the channel between source and drain electrodes; (5) blow-drying the *n*-hexane layer; and (6) preparing the gold (Au) source–drain electrodes (50 nm) *via* thermal-vacuum evaporation, with the fibers acting as the mask. Finally, an additional metal mask with large dimensions is constructed, with no real requirements in terms of form and precision: its main purpose is to fabricate the source/drain electrodes with a certain width and improve the manufacturing efficiency.

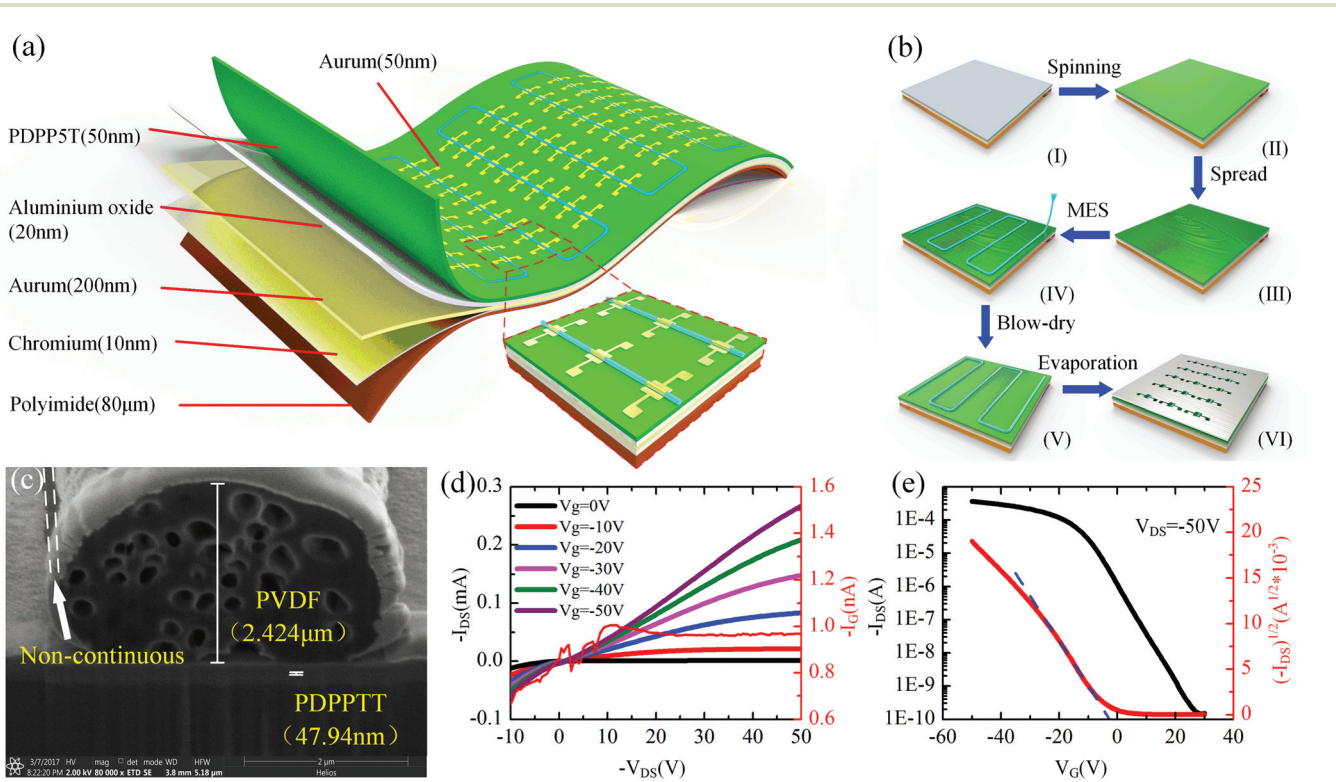


**Fig. 1** (a) Schematic of a large-area TFT array on a flexible substrate, the inset figure is partial enlarged drawing. (b) The schematic diagram of the manufacturing process. (c) The cross-section geometry of the transistor with a PVDF fibre after metal deposition process by the SEM. (d) and (e) Output current–voltage and transfer plots of one device, respectively.

Fig. 1c is a scanning electron microscopy (SEM) image of the cross-section of a PVDF fiber after metal deposition process by thermal vacuum evaporation: it can be observed that that there is no contact between the metal film upon the fiber and the metal film on the semiconductor layer.

The thickness of the semiconductor layer is 47.94 nm, which aligns with the experimental parameters. The diameter of the fiber used to form the source/drain channel is ~2.5 μm. Fig. 1d and e show that the transistor has a maximum mobility of 0.62 $cm^2\ V^{-1}\ s^{-1}$, with an impressive on/off current ratio of $2.47 \times 10^6$. The procedure described can be directly applied to flexible substrates, *e.g.*, PI/PET films, obtaining TFT arrays that are potentially useful within wearable electronic devices.

### Programmable fabrication of micro/nanochannels

Our proposed MES direct-writing method[37] uses a mechanical focused drawing force and distributed electrical field force to stretch the jet and is used to form micro/nanofibers masks with tunable dimensions.[38,39] This technique also uses a short nozzle-to-substrate distance to improve positioning *via* a high-speed moving stage. However, the incoming liquid jets on the substrate will form a ribbon rather than a perfect fiber because of the lack of evaporation of the solvent, owing to the small distance between nozzle and substrate. To solve this problem, a layer of *n*-hexane was spin-coated on to the receiving substrate before the MES direct-writing, and well-formed fibers were obtained once the *n*-hexane completely evaporated. The pattern, diameter, and position of the deposited fiber can simply be controlled by varying process parameters such as the nozzle-to-substrate distance ($H$), the applied voltage ($U$), the fluid supply ($Q$) and the velocity of the substrate ($v$).

Fig. 2a shows the in-house developed MES direct-writing equipment (Me-Jet Printer), which consists of the X–Y moving stage, the DC power supplier connecting the nozzle and the ground collector, the solution supply system, consisting of a syringe pump and syringe, a real-time observation system (a high-speed camera to view the jet-stream). Fig. 2b–e demonstrate the feasibility of the process in forming large-area lattice fibers. The uniformity of the fibers can be attributed to the programmable resolution. Controlling the moving stage along a given track at 400 mm $s^{-1}$ was carried out by a cross-shaped microfiber network with a 150 μm gap, which could be direct-written as shown in Fig. 2b (the local enlarged drawing is shown in the upper inset graph of Fig. 2b). Fig. 1c and the bottom inset graph of Fig. 2b reveal that the fibers were almost fully solidified with a diameter of 2.5 μm and 1 μm, respectively. The experimental results (Fig. 2c and d) demonstrate that the diameter of the microfiber increases linearly with the applied voltage and the fluid supply. The electric field and the flying time of the jet-stream were both changed when the

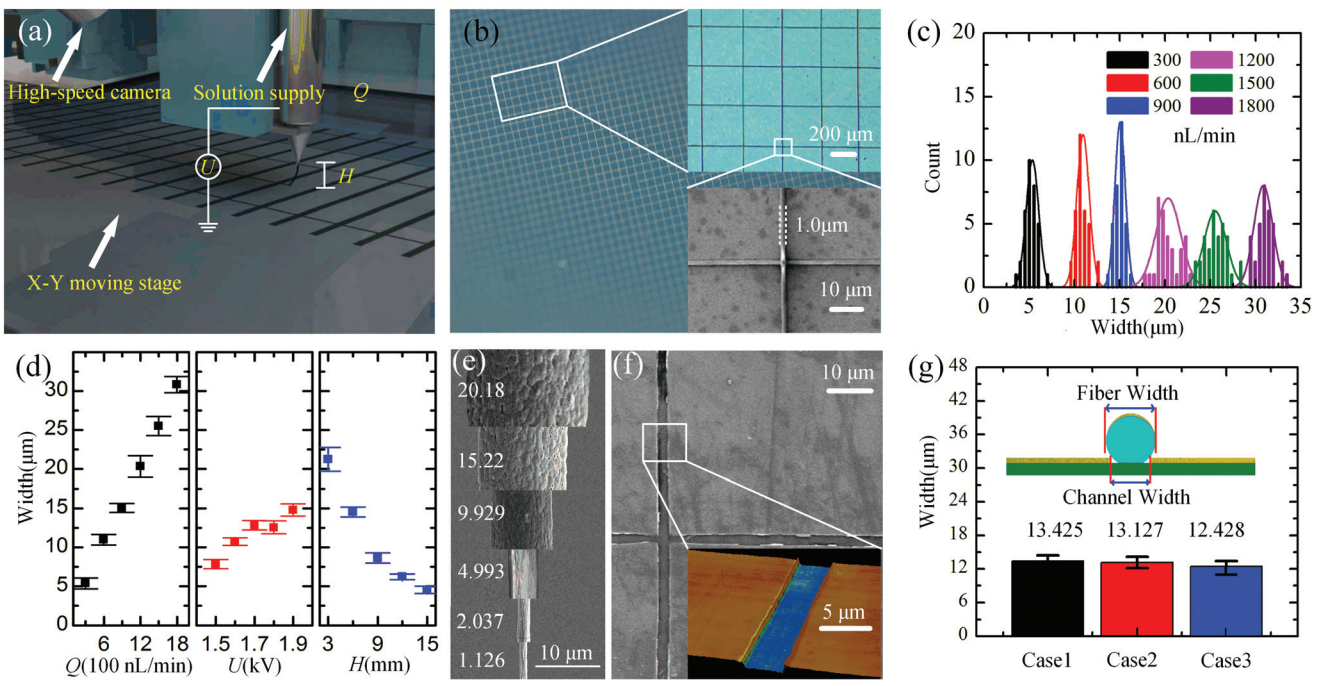


**Fig. 2** The fabrication process of microfiber array. (a) The physical map of the self-developed equipment (ME-Jet Printer). (b) Optical picture of latticed fibers on Si substrate with 150 μm gap examined with laser scanning confocal microscopy (LSCM, KEYENCE VK-X200K). Inset SEM images show the morphology of the intersection of two PVDF fibers. (c) The normal distribution of fiber diameter with different flow supply varied from 300 nL $min^{-1}$ to 1800 nL $min^{-1}$ at substrate speed of 200 mm $s^{-1}$ with 3 mm nozzle-to-substrate distance. (d) The SEM images of uniform and continuous microfibers with diameter regulating from 30 μm to 1 μm. (e) The SEM images demonstrated the formation of uniform and continuous microfibers with the diameter ranging from 20 μm to 1 μm. (f) The SEM image of micro/nanochannel with 4 μm and the inset 3D graph was examined by LSCM (g) The diameter of the fiber without evaporation (Case 1), the one with evaporation (Case 2) and the channel width after removing the fiber (Case 3).

nozzle-to-substrate distance varied; hence, the diameter of the microfiber reduced nonlinearly with the distance. The experimental data provided significant statistical characteristics of a normal distribution and the value of the coefficient of variation was below 6.7% when only one of the three parameters changed. The diameter could be precisely tuned from 20 μm to 1 μm, and SEM showed the formation of uniform and continuous microfibers (Fig. 2e).

The micro/nanochannels were obtained on the substrate (Fig. 2f and the inset graph) where the fibers functioned as a mask during thermal vacuum evaporation before removal. However, the channel width will be slightly less than the diameter of the fiber because of the scattering experienced during thermal vacuum evaporation. Fig. 2g shows the diameter of the fiber before and after thermal evaporation, and the channel width after removing the fiber, and the deviation between them [$\delta$ = (13.425–12.428)/13.425 × 100% ≈ 7.4%] is less than 10%; thus, the channel dimension can be regarded as the diameter of the fiber in our research.

### Performance of the micro/nanochannel TFT device

The characteristics of a PDPP5T[40] transistor array on octadecyltrichlorosilane (OTS-18)-treated Si/$SiO_2$ substrates were investigated using a bottom-gate, top-contact structure. The fabrication and evaluation were conducted under ambient conditions without taking precautionary measures to exclude atmospheric oxygen, moisture, and light. Since the channel layers are all connected to each other as a film, parasitic effects influence the performance of the OTFTs due to the lack of channel isolation (ESI Fig. S1†). However, the effects are limited, and hence the performance with the channels not isolated can be directly used as the experiment results.

The channel length ($L$) and width ($W$) have a significant impact on the performance of the devices according to $I_{DS} = \mu WC_i (V_G - V_T)^2/2L$; therefore, microfibers with a different diameter and a stainless steel reticle of different sizes were utilized to fabricate TFTs. Fig. 3a shows that the $I_{DS}$ was inversely proportional to the channel length, although the mobility of the device remained the same, in the order $10^{-1}$ $cm^2$ $V^{-1}$ $s^{-1}$. At the same time, the contact resistance ($R_c$) and channel resistance ($R_{ch}$) of transistors were investigated to better understand the transport properties. $R_c$ and $R_{ch}$ were extracted from the total resistance ($R_{total} = V_{DS}/I_{DS} = R_{ch} \times L + R_c$).[41,42] The resistances of all five devices measured less than 50 kΩ, and the minimum value reached 24.5 kΩ, with the channel length of 1.2 μm, demonstrating that the process can guarantee a small contact resistance (a detailed discussion is provided in ESI Fig. S2 and text S1†). A steel hollow mask corresponding to

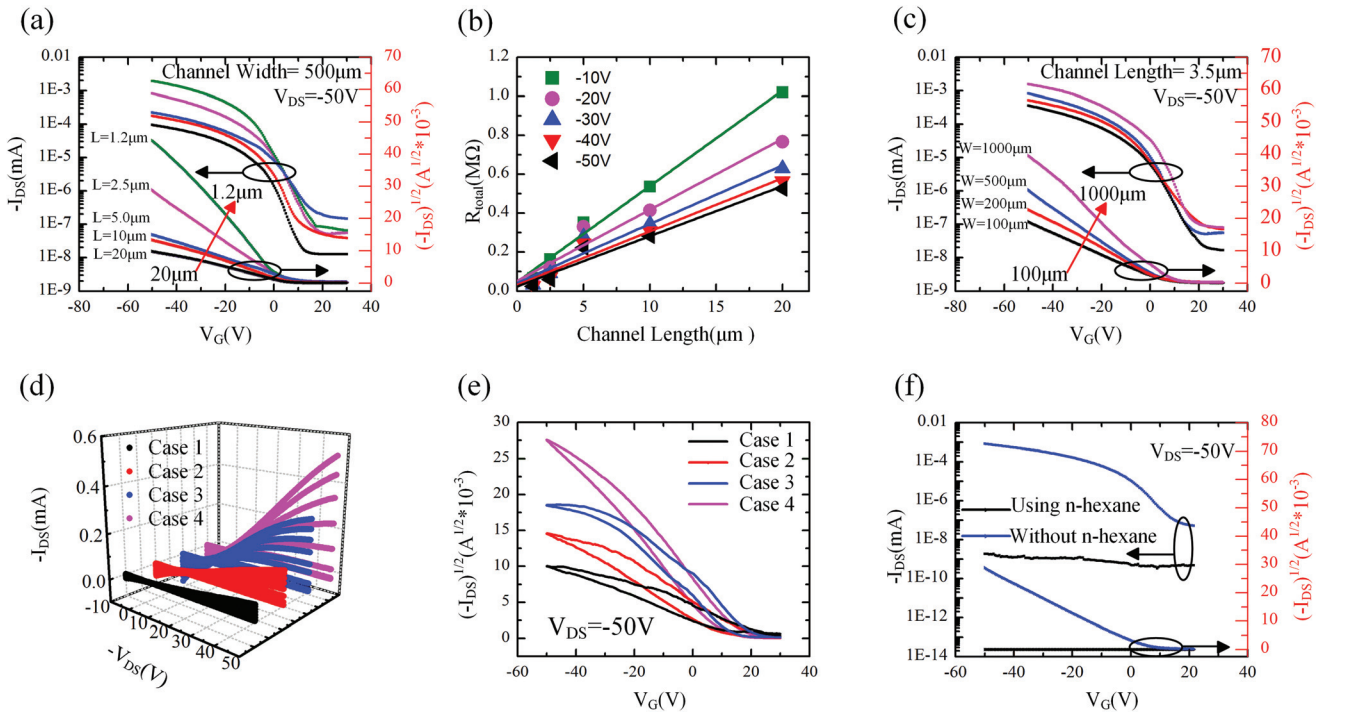


**Fig. 3** TFT performance characteristics. (a) Transfer characteristics of devices with different channel lengths at source/drain voltage ($V_{DS}$) of −50 V showing dependence of $(I_{DS})^{1/2}$–$V_G$ plot on channel length. (b) Plots of $R_{total}$ *vs.* channel length for OTFTs with $V_G$ varing from −10 to −50 V in the linear region ($V_{DS}$ = −50 V). (c) Transfer characteristics of devices with different channel widths at source/drain voltage ($V_{DS}$) of −50 V showing dependence of $(I_{DS})^{1/2}$–$V_G$ plot on channel width. (d) Output characteristics of TFT with different interface processing and annealing treatment (channel length = 5 μm, channel width = 500 μm, $V_G$ = −50 V), case 1–4 represent annealing twice without OTS, annealing twice with OTS, no annealing with OTS and annealing twice with OTS. (e) Transfer characteristics of the device corresponding to the above figure, case 1–4 represent annealing twice without OTS, annealing twice with OTS, no annealing with OTS and annealing twice with OTS. (f) Transfer characteristics of devices whether the substrate was treated with hexane or not before the electrospinning at source/drain voltage ($V_{DS}$) of −50 V.

the channel length with dimensions ranging from 100 μm to 1000 μm, was employed to obtain transistors with different channel widths. Fig. 3c shows that the $I_{DS}$ was proportional to the channel width. However, the mobility remained in the same order of magnitude.

At the same time, a series of related experiments were performed to demonstrate the uniformity of the TFT array for large-area fabrication. The specific data are shown in the ESI Table S1,† and summarized in ESI Fig. S3.† These data demonstrate that the transistors prepared by the mechano-electrospinning method have a good stability.

Besides the size factors, the modification between the semiconductor and the insulating layer and times of annealing also affected the final performance of TFT devices. OTS-18 was selected to modify the layer, and the device could be annealed after spin-coating the semiconductor solution and before testing the transistor. The output and transfer characteristics are shown in Fig. 3d and e with four combinations. As expected, the TFT with the modified layer had a higher hole-mobility and high on/off current ratio than the one without OTS. When the device fabricated on OTS-18-treated $Si/SiO_2$ substrates and annealed once after spin-coating the PDPP5T is compared with the one without annealing, it was found that the former outperformed the latter. However, if the device was annealed once more before testing, the fiber with the organic solvent residue would shrink sharply and tear the layer of the semiconductor. Thus, the performance of the transistor would decrease significantly as shown.

In addition, it is worth noting that incorporating a layer of *n*-hexane on the receiving substrate, followed by MES direct-writing, was crucial to ensuring the successful manufacturing of a well-functioning device. Without the layer, the microfiber would not be completely cured, and then not only would the solvent have a doping effect on the semiconductor but the semiconductor layer would also experience damage when the fiber would be removed to test for the ribbon having a strong adhesion with the PDPP5T, resulting in the loss of characteristics of the transistor, as shown in Fig. 3f.

The stability of the TFTs was then tested by varying the testing cycles and time, the voltage between the source and drain electrodes, and the external light concentrated on the TFT devices. The BGTC devices on OTS-18 treated $Si/SiO_2$ substrate displayed excellent operating cyclic stability as it maintained the on- and off-currents very well when turned on and off continuously over 1200 cycles (see the inset figure of Fig. 4a). For devices stored in ambient conditions without insulation from atmospheric air, moisture and room light, it is anticipated that the semiconductor would be doped by vapor in the air, resulting in a slight rise of off-currents. By means of the transfer plots, it can be seen that the on/off ratio was between $10^5$ and $10^6$ and the hole mobility fluctuated at around 0.4 $cm^2\ V^{-1}\ s^{-1}$ (Fig. 4a). The same devices were used

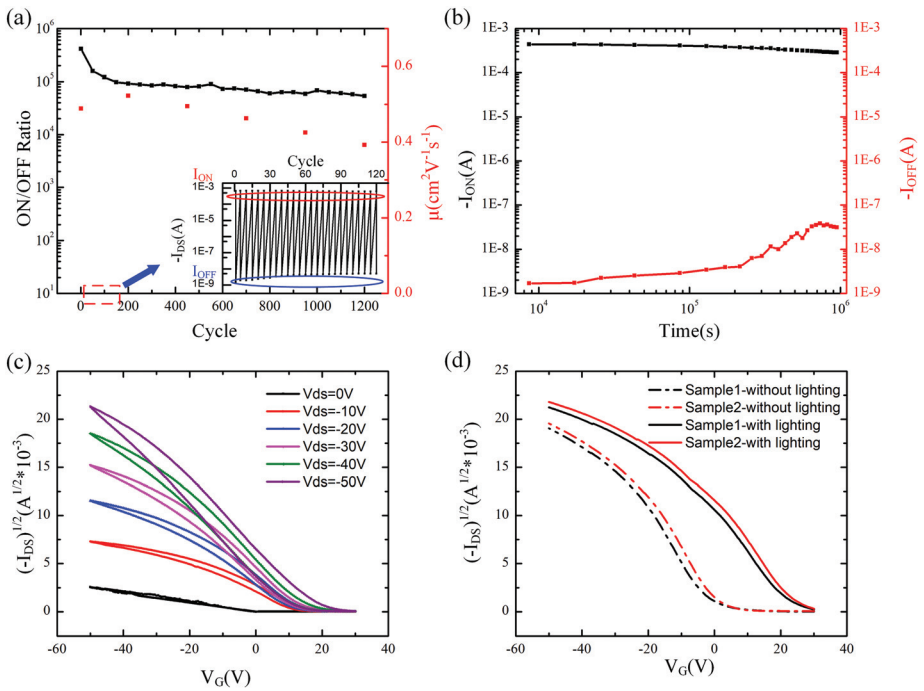


**Fig. 4** TFT performance characteristics under different testing conditions. (a) Cyclic stability of a representative device showing maintenance of on- and off-currents during continuous on/off cycles. The inset figure shows the on/off-currents of the device during the 0–120 cycles. (b) Shelf-life stability under ambient conditions, showing stability of mobility and on/off ratio obtained from ten representative devices for two weeks. (c) Transfer characteristics of a device (channel length = 5 μm, $W$ = 500 μm) under different $V_{DS}$ showing dependence of $(I_{DS})^{1/2}$–$V_G$ plot on source/drain field. (d) Transfer characteristics of two separate device (channel length = 5 μm, $W$ = 500 μm) with external light or not showing dependence of $(I_{DS})^{1/2}$–$V_G$ plot on source/drain field.

 

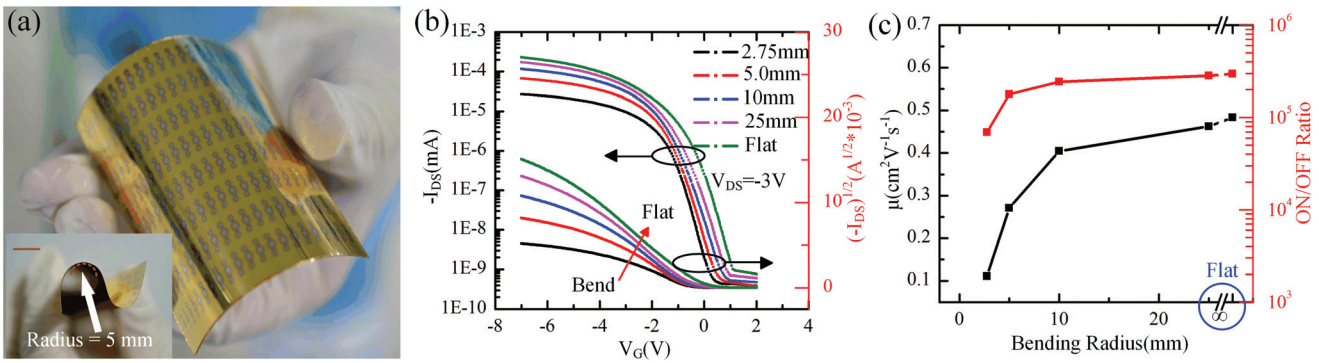


**Fig. 5** TFT performance characteristics of OTFT devices on the PI substrate. (a) The photographic image of the flexible TFTs array on the PI substrate. The bending radius of devices in the inset graph is 5 mm and the scale bar is 10 mm. (b) Transfer characteristics of devices with different bending radius at source/drain voltage ($V_{DS}$) of −3 V showing dependence of $(I_{DS})^{1/2}$–$V_G$ plot on bending radius. (c) The mobility and ON/OFF ratio of the flexible transistors under different bending status.

to monitor the lifetimes of OTFTs. The mobility and on/off ratio of five representative devices were measured periodically over a period of two weeks. Fig. 4b shows the on- and off-currents of the devices: no significant fluctuations were observed under ambient conditions over seven days. These results demonstrate that transistors with stable performance can be prepared using the process outlined in this study. Fig. 4c shows how the output current can be regulated by the voltage between the source and drain electrodes; however, a distinct hysteresis effect was noted, which may be caused by the organic solvent in the microfiber, resulting in the structural defects of the semiconductor film. Interestingly, the on-currents of the devices could be controlled visibly with external light (Fig. 4d). Through the testing of the samples, it is clear that the $I_{DS}$ is proportional to the intensity of the applied light, which implies that the devices have the potential to be used as photodetectors.[43]

### Flexible TFT device

Fig. 5a shows an optical image of the flexible TFT array. The PDPP5T transistors were fabricated on an 80 μm-thick PI substrate coated with 10 nm Cr and 200 nm Au as the bottom gate electrode. Then, an aluminum oxide layer with 20 nm thickness is deposited by ALD to form the insulator. After spin-coating and annealing the semiconductor PDPP5T (50 nm), the micro/nanofibers were directly printed and the gold (Au) source–drain electrodes were prepared *via* thermal-vacuum evaporation [note that the gold (Au) source–drain electrodes were replaced with platinum (Pt) for taking a photograph]. The representative transfer curves ($I_{DS}$–$V_{GS}$) of the fabricated device whilst being deformed (by bending) were plotted against the different bending radii (Fig. 4b). Upon bending the device from 25 mm to 2.75 mm, the electronic performance was stable with only a slight reduction in $I_{ON}$ and hole mobility. With regards to the relative permittivity of the aluminum oxide (6.5), the changes in the relative values of $\mu$ and the on/off current ratio were monitored as a function of the bending radius (shown in Fig. 5c), with slight variations when the radius is over 2.75 mm. The mobility and the on/off ratio decrease with applied strain. It is anticipated that further bending of the substrate would degrade the electronic performance dramatically until the elastic limit of aluminum oxide; this would fragment aluminum oxide and the semiconductor layer would subsequently be destroyed. Therefore, flexible transistors of this nature (and at this level of development) can only be applied to wearable electronic devices for low open and operating voltages.

## Conclusion

We have proposed a simple MES direct-writing process as an alternative to lithography for fabricating large-area, flexible, small-channel TFTs. The TFT devices fabricated with PDPP5T exhibit high mobilities (up to 0.62 cm$^2$ V$^{-1}$ s$^{-1}$) and on/off ratios (>10$^6$) and have operational stabilities with long lifetimes. When the devices were extended to flexible transistor arrays, they maintained reliable electrical and mechanical stability. When in combination with 30 nm $Al_2O_3$ gate dielectrics, 100 μm PI substrates enable the entire transistor arrays to have a bending radius of 2.75 mm. This work opens a new way to fabricate flexible electronic devices by a mask-less process.

## Experimental

### Materials

The PDPP5T solution was prepared by dissolving PDPP5T (4 mg ml$^{-1}$, synthesized according to our reported method[38]) in dichlorobenzene (Sigma Aldrich Inc.) by heating to 70 °C. PVDF (Kynar 761, Arkema Investment Co. Ltd) was dissolved in 3 : 2 volume ratio of dimethylformamide/acetone (DMF/acetone, Sigma Aldrich) at a polymer/solvent concentration of 18% w/w, and heated at 40 °C for 4 h to make the solution homogeneous.

### MES directing-writing and electron microscopy

MES direct-writing was performed by placing 0.5 ml of solution into a 1.0 ml plastic syringe tipped with a 25-gauge stainless steel needle (inner diameter 260 mm and external diameter 520 mm). The nozzle is also used as an electrode and connected with a current power supplier (digital function generator Agilent_33500_Series by Agilent Inc., and amplifier TREK++609E-6 from TREK Inc.). The ground collector is a metal plate with 3 mm thickness and is fixed on a moving stage. The solution is delivered through plastic pipes using a syringe pump (Pump 11 Elite Nanomite, HARVARD, Inc.). A high-speed camera (industrial camera acA2000-340 km, Basler Inc.) is used to observe the motion of the jet. The X–Y moving stage is designed in-house (X–Y linear motor stage and the programmable controller is Parker Inc. production). The substrate is mounted on the ground collector beneath the nozzle. The nozzle-to-substrate distance varied from 1 to 30 mm. The electrospun fibers were examined using laser scanning confocal microscopy (LSCM, KEYENCE VK-X200K). The SEM pictures are captured after sputtering a gold film on the pattern.

### Fabrication of TFT devices

A heavily n-doped Si wafer with a 300 nm $SiO_2$ surface layer (capacitance of 11.5 nF $cm^{-2}$) was employed as the substrate with a Si wafer serving as a common gate electrode and $SiO_2$ as the dielectric. For convenience, the Si wafer was cut into 1 cm × 1 cm squares. For the OTS-18 SAM modification, the Si wafer surface was first immersed in Piranha solution (7 : 3 mixture of sulfuric acid and 30% hydrogen peroxide) for 10 min. This was followed by rinsing with deionized water several times. It was then sonicated sequentially in isopropyl alcohol, ethanol and acetone for 6 min each, and then rotated inside a culture disk with a drop of octadecyltrichlorosilane (OTS-18) in the middle. The disk was then covered and heated in a vacuum oven at 120 °C for 2 h, resulting in the formation of an OTS-18 SAM on the surface. The Si wafer surface was cleaned twice by sonication – sequentially in hexane, trichloromethane and isopropyl alcohol for 10 min each, and was then blown-dried with nitrogen. For BGTC devices, the semiconductor was spin-coated from its dichlorobenzene solution (4 mg $ml^{-1}$) onto the dielectric surface at 2000 rpm for 60 s, before being annealed in a vacuum oven at 200 °C for 10 min. The microfiber array was deposited on the Si wafer followed by adding *n*-hexane solution to form a liquid film on the substrate. The Au source/drain electrodes were then deposited *via* thermal-vacuum evaporation on the semiconductor layer, with the fibers acted as the mask bearing source/drain electrode features of various dimensions. The fabrication of TFT on flexible PI substrates was performed under ambient conditions (except for the deposition of the Au electrodes). 10 nm Cr and 200 nm Au gate electrodes were deposited on the substrate *via* thermal vacuum evaporation. The substrate was then deposited with a 30 nm $Al_2O_3$ dielectric layer by ALD. Thereafter, the semiconductor layer, fiber array and the Au source/drain electrodes were fabricated, as mentioned previously.

### Device characterization

Characterization of fabricated OTFT devices was carried out using a Keithley 4200 Semiconductor Characterization System under ambient conditions. The field-effect mobility in the saturation regime was extracted using the equation: $I_{DS} = \mu WC_i (V_G - V_T)^2/2L$, under the condition of $-V_{DS} > -(V_G - V_T)$. For mobility in the linear regime, the equation, $I_{DS} = \mu WC_i (V_G - V_T - V_{DS}/2)/2L$ was applied under the condition: $-V_{DS} \leq -(V_G - V_T)$, where $I_{DS}$ is the source–drain current, $\mu$ is the field-effect mobility, $W$ is the channel width, $L$ is the channel length, $C_i$ is the capacitance per unit area of gate dielectric layer, $V_G$ and, $V_T$ and $V_{DS}$ are the gate, threshold and source–drain voltages, respectively.

## Conflicts of interest

There are no conflicts to declare.

## Acknowledgements

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