FSV9504

ICODE and ISO/IEC 15693 reader IC

Rev. 1.0 — 10 March 2014 **Product data sheet**

1. Introduction

This data sheet describes the functionality of the FSV9504 Integrated Circuit (IC). It includes the functional and electrical specifications and from a system and hardware viewpoint gives detailed information on how to design-in the device.

2. General description

The FSV9504 is a member of a new family of highly integrated reader ICs for contactless communication at 13.56 MHz. This family of reader ICs provide:

- outstanding modulation and demodulation for passive contactless communication
- a wide range of methods and protocols

The transmitter module Section 8.9 on page 24 can directly drive an antenna designed for proximity operating distance up to 100 mm without additional active circuitry. The receiver module provides a robust and efficient demodulation/decoding circuitry implementation for compatible transponder signals (see Section 8.10 on page 28).

All layers of the ICODE1 and ISO/IEC 15693 protocols are supported. The receiver module provides a robust and efficient demodulation/decoding circuitry implementation for ICODE1 and ISO/IEC 15693 compatible transponder signals. The digital module manages ICODE1 and ISO/IEC 15693 framing and error detection (CRC).

A parallel interface can be directly connected to any 8-bit microprocessor to ensure reader/terminal design flexibility.

3. Features and benefits

3.1 General

Highly integrated analog circuitry for demodulating and decoding label response
Buffered output drivers enable antenna connection using the minimum of external
Proximity operating distance up to 100 mm
Parallel microprocessor interface with internal address latch and IRQ line

Supports both ICODE1 and ISO/IEC 15693 protocols
components

Flexible interrupt handling

Automatic detection of parallel microprocessor interface type

64-byte send and receive FIFO buffer
Hard reset with low power function
Compatible with the SLRC400

Software controlled Power-down mode
Programmable timer
Unique serial number
User programmable start-up configuration
Bit-oriented and byte oriented framing
Independent power supply pins for analog, digital and transmitter modules
Internal oscillator buffer optimized for low phase jitter enables 13.56 MHz quartz connection
3.3 V operation for transmitter (antenna driver) in short range and proximity applications

4. Applications

Electronic payment systems
Identification systems
Access control systems
Subscriber services
Banking systems
Digital content systems

5. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
FSV9504	SO32	plastic small outline package; 32 leads; body width 7.5 mm	SOT287-1

6. Block diagram

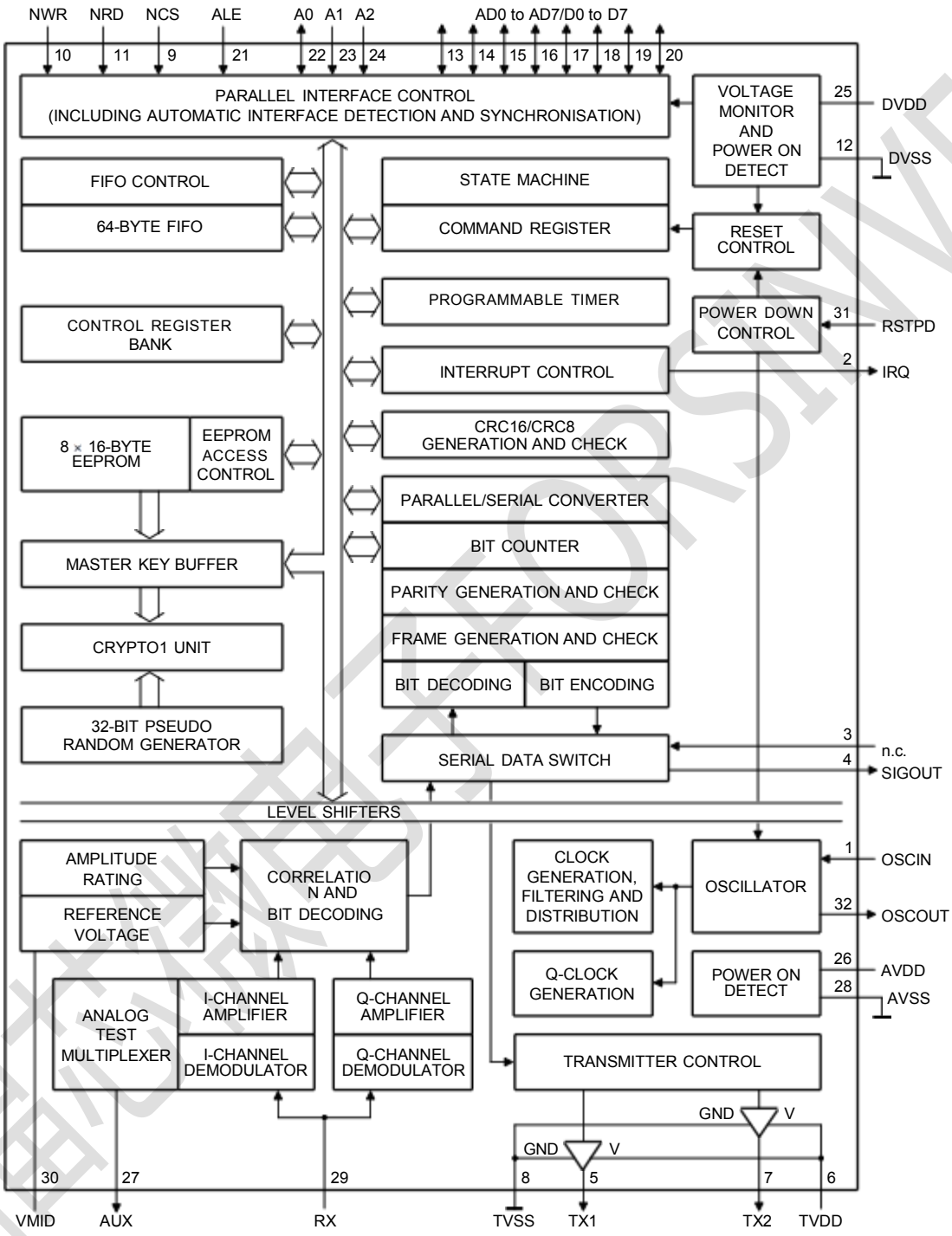


Fig 1. FSV9504 block diagram

7. Pinning information

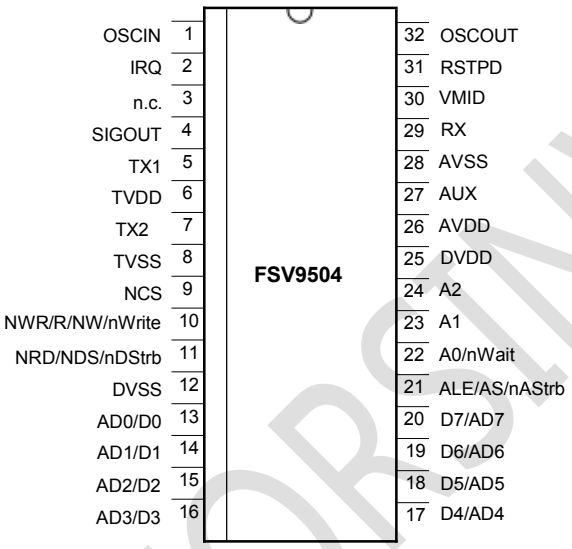


Fig 2. FSV9504 pin configuration

7.1 Pin description

Table 2. Pin description

Pin	Symbol	Type[1]	Description
1	OSCIN	I	oscillator or clock input: crystal oscillator input to the oscillator's inverting amplifier externally generated clock input; f_{osc} = 13.56 MHz
2	IRQ	O	interrupt request output signals an interrupt event
3	n.c.	I	connect this pin to ground
4	SIGOUT	O	ICODE interface serial data output based on ICODE1 and ISO/IEC 15693
5	TX1	O	transmitter 1 modulated carrier output; 13.56 MHz
6	TVDD	P	power supply for transmitter output stage pins TX1 and TX2
7	TX2	O	transmitter 2 modulated carrier output; 13.56 MHz
8	TVSS	G	transmitter ground for the TX1 and TX2 output stages
9	NCS	I	not chip select input selects and activates the FSV9504's microprocessor interface
10[2]	NWR	I	not write input strobe signal for writing data to the FSV9504 registers when applied to pins D0 to D7
	R/NW	I	read not write input indicates that a read or a write cycle must be performed
	nWrite	I	not write input indicates that a read or a write cycle must be performed
11[2]	NRD	I	not read input strobe signal for reading data from the FSV9504 registers when applied to pins D0 to D7
	NDS	I	not data strobe input strobe signal for read and write cycles
	nDStrb	I	not data strobe input strobe signal for read and write cycles

Table 2. Pin description

Pin	Symbol	Type[1]	Description
12	DVSS	G	digital ground
13 to 20[2]	D0 to D7	I/O	8-bit bidirectional data bus input/output on pins D0 to D7
	AD0 to AD7	I/O	8-bit bidirectional address and data bus input/output on pins AD0 to AD7
21[2]	ALE	I	address latch enable input for pins AD0 to AD5; HIGH latches the internal address
	AS	I	address strobe input for pins AD0 to AD5; HIGH latches the internal address
	nAStrb	I	not address strobe input for pins AD0 to AD5; LOW latches the internal address
22[2]	A0	I	address line 0 is the address register bit 0 input
	nWait	O	not wait output: LOW starts an access cycle HIGH ends an access cycle
23	A1	I	address line 1 is the address register bit 1 input
24	A2	I	address line 2 is the address register bit 2 input
25	DVDD	P	digital power supply
26	AVDD	P	analog power supply for pins OSCIN, AUX, RX, VMID and OSCOUT
27	AUX	O	auxiliary analog test signal output. The output signal is selected using the TestAnaSelect register's TestAnaOutSel[4:0] bits
28	AVSS	G	analog ground
29	RX	I	receiver input for the label response. The carrier is load modulated at 13.56 MHz, taken from the antenna circuit
30	VMID	P	internal reference voltage: provides the internal reference voltage as a supply **Remark:** It must be connected to ground using a 100 nF block capacitor.
31	RSTPD	I	reset and power-down input: HIGH: switches off the internal current sinks, inhibits the oscillator and disconnects the input pads LOW (negative edge): starts the internal reset phase
32	OSCOUT	O	crystal oscillator output for the oscillator's inverting amplifier

[1] Pin types: I = Input, O = Output, I/O = Input/Output, P = Power and G = Ground.

[2] These pins provide different functionality depending on the selected microprocessor interface type (see Section 8.1 on page 6 for detailed information).

8. Functional description

8.1 Digital interface

8.1.1 Overview of supported microprocessor interfaces

The FSV9504 supports direct interfacing to various 8-bit microprocessors. Alternatively, the FSV9504 can be connected to a PC's Enhanced Parallel Port (EPP). Table 3 shows the parallel interface signals supported by the FSV9504.

Table 3. Supported microprocessor and EPP interface signals

Bus control signals	Bus	Separated address and data bus	Multiplexed address and data bus
Separated read and write strobes	control	NRD, NWR, NCS	NRD, NWR, NCS, ALE
	address	A0, A1, A2	AD0, AD1, AD2, AD3, AD4, AD5
	data	D0 to D7	AD0 to AD7
Common read andwrite strobe	control	R/NW, NDS, NCS	R/NW, NDS, NCS, AS
	address	A0, A1, A2	AD0, AD1, AD2, AD3, AD4, AD5
	data	D0 to D7	AD0 to AD7
Common read and write strobe with handshake (EPP)	control	-	nWrite, nDStrb, nAStrb, nWait
	address	-	AD0, AD1, AD2, AD3, AD4, AD5
	data	-	AD0 to AD7

8.1.2 Automatic microprocessor interface detection

After a Power-On or Hard reset, the FSV9504 resets parallel microprocessor interface mode and detects the microprocessor interface type.

The FSV9504 identifies the microprocessor interface using the logic levels on the control pins after the reset phase. This is performed using a combination of fixed pin connections and the dedicated Initialization routine (see Section 8.7.4 on page 23).

8.1.3 Connection to different microprocessor types

The connection to various microprocessor types is shown in Table 4.

Table 4. Connection scheme for detecting the parallel interface type

FSV9504 pins	Parallel interface type and signals				
	Separated read/write strobe		Common read/write strobe		
	Dedicated address bus	Multiplexed address bus	Dedicated address bus	Multiplexed address bus	Multiplexed address bus with handshake
ALE	HIGH	ALE	HIGH	AS	nAStrb
A2	A2	LOW	A2	LOW	HIGH
A1	A1	HIGH	A1	HIGH	HIGH
A0	A0	HIGH	A0	LOW	nWait
NRD	NRD	NRD	NDS	NDS	nDStrb
NWR	NWR	NWR	R/NW	R/NW	nWrite
NCS	NCS	NCS	NCS	NCS	LOW
D7 to D0	D7 to D0	AD7 to AD0	D7 to D0	AD7 to AD0	AD7 to AD0

8.1.3.1 Separate read and write strobe

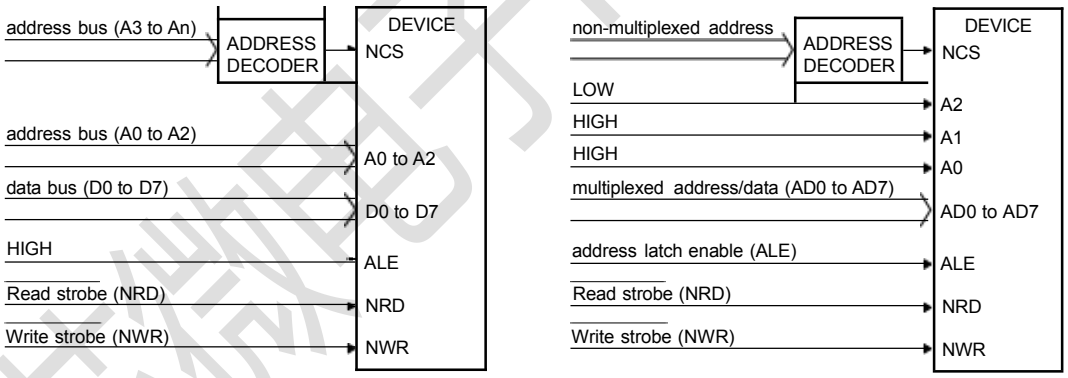


Fig 3. Connection to microprocessor: separate read and write strobes

Refer to Section 12.4.1 on page 80 for timing specification.

8.1.3.2 Common read and write strobe

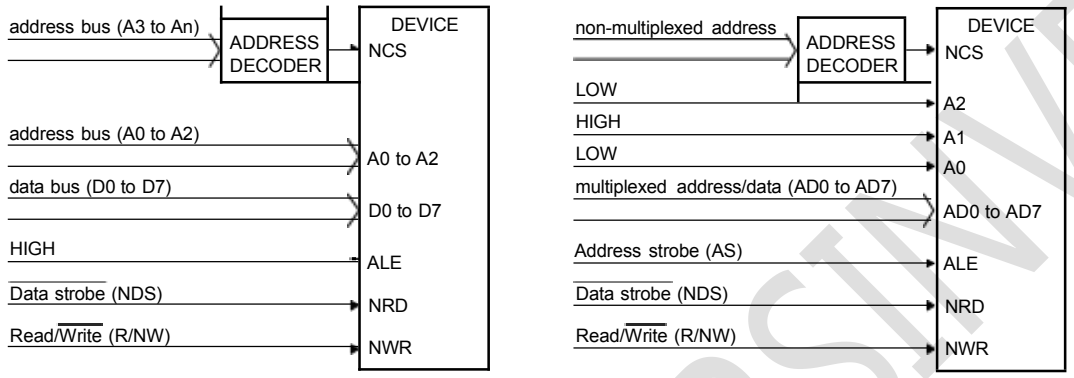


Fig 4. Connection to microprocessor: common read and write strobes

Refer to Section 12.4.2 on page 81 for timing specification.

8.1.3.3 Common read and write strobe: EPP with handshake

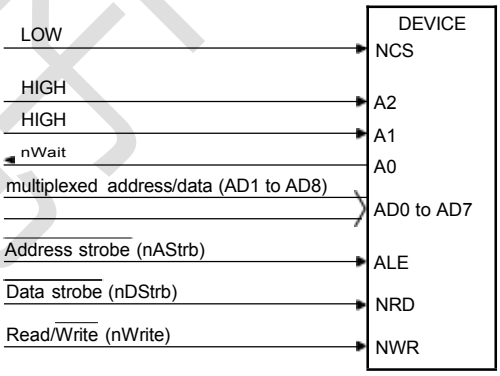


Fig 5. Connection to microprocessor: EPP common read/write strobes and handshake

Refer to Section 12.4.3 on page 82 for timing specification.

Remark: In the EPP standard a chip select signal is not defined. To cover this situation, the status of the NCS pin can be used to inhibit the nDStrb signal. If this inhibitor is not used, it is mandatory that pin NCS is connected to pin DVSS.

Remark: After each Power-On or Hard reset, the nWait signal on pin A0 is high-impedance. nWait is defined as the first negative edge applied to the nAStrb pin after the reset phase. The FSV9504 does not support Read Address Cycle.

8.2 Memory organization of the EEPROM

Table 5. EEPROM memory organization diagram

Block		Byte address	Access	Memory content	Refer to
Position	Address				
0	0	00h to 0Fh	R	product information field	Section 8.2.1 on page 9
1	1	10h to 1Fh	R/W	StartUp register initialization file	Section 8.2.2.1 on page 10
2	2	20h to 2Fh	R/W		
3	3	30h to 3Fh	R/W	register initialization file	Section 8.2.2.3 “Register initialization file (read/write)” on page 12
4	4	40h to 4Fh	R/W		
5	5	50h to 5Fh	R/W	user data or second initialization	
6	6	60h to 6Fh	R/W		
7	7	70h to 7Fh	R/W		

Remark: It is recommend to use only the above EEPROM address area.

8.2.1 Product information field (read only)

Table 6. Product information field byte allocation

Byte	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	CRC	RsMaxP	Internal		Product Serial Number				Reserved			Product Type Identification				
Access	R	R	R		R				R			R				

Table 7. Product information field

Byte	Symbol	Access	Value	Description
15	CRC	R	-	the content of the product information field is secured using a CRC byte which is checked during start-up
14	RsMaxP	R		maximum source resistance for the p-channel driver transistor on pins TX1 and TX2 The source resistance of the p-channel driver transistors of pin TX1 and TX2 can be adjusted using the value GsCfgCW[5:0] in the CwConductance register (see Section 8.9.3 on page 25). The mean value of the maximum adjustable source resistance for pins TX1 and TX2 is stored as an integer value in Ω in this byte. Typical values for RsMaxP are between 60 Ω to 140 Ω. This value is denoted as maximum adjustable source resistance $R_{S(ref)maxP}$ and is measured by setting the CwConductance register’s GsCfgCW[5:0] bits to 01h.
13 to 12	Internal	R		two bytes for internal trimming parameters
11 to 8	Product Serial Number	R	-	a unique four byte serial number for the device
7 to 5	reserved	R		
4 to 0	Product Type Identification	R	-	the FSV9504 is a member of a new family of highly integrated reader ICs. Each member of the product family has a unique product type identification. The value of the product type identification is shown in Table 8.

Table 8. Product type identification definition

Definition	Product type identification bytes				
Byte	0	1	2	3	4[1]
Value	30h	33h	F1h	00h	XXh

[1] Byte 4 contains the current version number.

8.2.2 Register initialization file (read/write)

Register initialization from address 10h to address 2Fh is performed automatically during the initializing phase (see Section 8.7.3 on page 23) using the StartUp register initialization file.

In addition, the FSV9504 registers can be initialized using values from the StartUp register initialization file when the LoadConfig command is executed (see Section 10.4.1 on page 75).

Remark: The following points apply to initialization:

- the Page register (addressed using 10h, 18h, 20h, 28h) is skipped and not initialized.
- make sure that all PreSetxx registers are not changed.
- make sure that all register bits that are reserved are set to logic 0.

8.2.2.1 StartUp register initialization file (read/write)

The EEPROM memory block address 1 and 2 contents are used to automatically set the register subaddresses 10h to 2Fh during the initialization phase. The default values stored in the EEPROM during production are shown in Section 8.2.2.2 “Factory default StartUp register initialization file”.

The byte assignment is shown in Table 9.

Table 9. Byte assignment for register initialization at start-up

EEPROM byte address	Register address	Remark
10h (block 1, byte 0)	10h	skipped
11h	11h	copied
…	…	…
2Fh (block 2, byte 15)	2Fh	copied

8.2.2.2 Factory default StartUp register initialization file

During the production tests, the StartUp register initialization file is initialized using the default values shown in Table 10. During each power-up and initialization phase, these values are written to the FSV9504’s registers.

Table 10. Shipment content of StartUp register initialization file

EEPROM byte address	Register address	Value	Symbol	Description
10h	10h	00h	Page	free for user
11h	11h	58h	TxControl	transmitter pins TX1 and TX2 are switched off, bridge driver configuration, modulator driven from internal digital circuitry
12h	12h	3Fh	CwConductance	source resistance of TX1 and TX2 is set to minimum
13h	13h	05h	ModGsCfg	source resistance of TX1 and TX2 at modulation to determine the modulation index
14h	14h	2Ch	CoderControl	selects the bit coding mode and framing during transmission
15h	15h	3Fh	ModWidth	pulse width for used code (1 out of 256 RZ or 1 out of 4); pulse coding is set to standard configuration
16h	16h	3Fh	ModWidthSOF	pulse width of Start Of Frame (SOF)
17h	17h	00h	PreSet17	-
18h	18h	00h	Page	free for user
19h	19h	8Bh	RxControl1	internal amplifier gain is maximum
1Ah	1Ah	00h	DecoderControl	bit-collisions always evaluate to HIGH in the data bit stream
1Bh	1Bh	54h	BitPhase	BitPhase[7:0] is set to standard configuration
1Ch	1Ch	68h	RxThreshold	MinLevel[3:0] and CollLevel[3:0] are set to maximum
1Dh	1Dh	00h	PreSet1D	-
1Eh	1Eh	41h	RxControl2	use Q-clock for the receiver, automatic receiver off is switched on, decoder is driven from internal analog circuitry
1Fh	1Fh	00h	ClockQControl	automatic Q-clock calibration is switched on
20h	20h	00h	Page	free for user
21h	21h	08h	RxWait	frame guard time is set to eight bit-clocks
22h	22h	0Ch	ChannelRedundancy	channel redundancy is set in accordance with ICODE1
23h	23h	FEh	CRCPresetLSB	CRC preset value is set in accordance with ICODE1
24h	24h	FFh	CRCPresetMSB	CRC preset value is set in accordance with ICODE1
25h	25h	00h	PreSet25	-
26h	26h	00h	SIGOUTSelect	pin SIGOUT is set LOW
27h	27h	00h	PreSet27	-
28h	28h	00h	Page	free for user
29h	29h	3Eh	FIFOLevel	WaterLevel[5:0] FIFO buffer warning level is set to standard configuration
2Ah	2Ah	0Bh	TimerClock	TPreScaler[4:0] is set to standard configuration, timer unit restart function is switched off
2Bh	2Bh	02h	TimerControl	Timer is started at the end of transmission, stopped at the beginning of reception
2Ch	2Ch	00h	TimerReload	TReloadValue[7:0]: the timer unit preset value is set to standard configuration
2Dh	2Dh	02h	IRQPinConfig	pin IRQ is set to high-impedance
2Eh	2Eh	00h	PreSet2E	-
2Fh	2Fh	00h	PreSet2F	-

8.2.2.3 Register initialization file (read/write)

The EEPROM memory content from block address 3 to 7 can initialize register sub addresses 10h to 2Fh when the LoadConfig command is executed (see Section 10.4.1 on page 75). This command requires the EEPROM starting byte address as a two byte argument for the initialization procedure.
The byte assignment is shown in Table 11.

Table 11. Byte assignment for register initialization at StartUp

EEPROM byte address	Register address	Remark
EEPROM starting byte address	10h	skipped
EEPROM + 1 starting byte address	11h	copied
	…	…
EEPROM + 31 starting byte address	2Fh	copied

The register initialization file is large enough to hold values for two initialization sets and up to one block (16-byte) of user data.

Remark: The register initialization file can be read/written by users and these bytes can be used to store other user data.

8.3 FIFO buffer

An 8 × 64 bit FIFO buffer is used in the FSV9504 to act as a parallel-to-parallel converter. It buffers both the input and output data streams between the microprocessor and the internal circuitry of the FSV9504. This makes it possible to manage data streams up to 64 bytes long without needing to take timing constraints into account.

8.3.1 Accessing the FIFO buffer

8.3.1.1 Access rules

The FIFO buffer input and output data bus is connected to the FIFOData register. Writing to this register stores one byte in the FIFO buffer and increments the FIFO buffer write pointer. Reading from this register shows the FIFO buffer contents stored at the FIFO buffer read pointer and increments the FIFO buffer read pointer. The distance between the write and read pointer can be obtained by reading the FIFOLength register.

When the microprocessor starts a command, the FSV9504 can still access the FIFO buffer while the command is running. Only one FIFO buffer has been implemented which is used for input and output. Therefore, the microprocessor must ensure that there are no inadvertent FIFO buffer accesses. Table 12 gives an overview of FIFO buffer access during command processing.

Table 12. FIFO buffer access

Active command	FIFO buffer		Remark
	µP Write	µP Read	
StartUp	-	-	
Idle	-	-	
Transmit	yes	-	
Receive	-	yes	

Table 12. FIFO buffer access

Active command	FIFO buffer		Remark
	µP Write	µP Read	
Transceive	yes	yes	the microprocessor has to know the state of the command (transmitting or receiving)
WriteE2	yes	-	
ReadE2	yes	yes	the microprocessor has to prepare the arguments, afterwards only reading is allowed
LoadConfig	yes	-	
CalcCRC	yes	-	

8.3.2 Controlling the FIFO buffer

In addition to writing to and reading from the FIFO buffer, the FIFO buffer pointers can be reset using the FlushFIFO bit. This changes the FIFOLength[6:0] value to zero, bit FIFOOvfl is cleared and the stored bytes are no longer accessible. This enables the FIFO buffer to be written with another 64 bytes of data.

8.3.3 FIFO buffer status information

The microprocessor can get the following FIFO buffer status data:

- the number of bytes stored in the FIFO buffer: bits FIFOLength[6:0]
- the FIFO buffer full warning: bit HiAlert
- the FIFO buffer empty warning: bit LoAlert
- the FIFO buffer overflow warning: bit FIFOOvfl.

Remark: Setting the FlushFIFO bit clears the FIFOOvfl bit.

The FSV9504 can generate an interrupt signal when:

- bit LoAlertIRq is set to logic 1 and bit LoAlert = logic 1, pin IRQ is activated.
- bit HiAlertIRq is set to logic 1 and bit HiAlert = logic 1, pin IRQ activated.

The HiAlert flag bit is set to logic 1 only when the WaterLevel[5:0] bits or less can be stored in the FIFO buffer. The trigger is generated by Equation 1:

$$HiAlert = 64 - FIFOLength \leq WaterLevel \quad (1)$$

The LoAlert flag bit is set to logic 1 when the FIFOLevel register's WaterLevel[5:0] bits or less are stored in the FIFO buffer. The trigger is generated by Equation 2:

$$LoAlert = FIFOLength \leq WaterLevel \quad (2)$$

8.3.4 FIFO buffer registers and flags

Table 13 shows the related FIFO buffer flags in alphabetical order.

Table 13. Associated FIFO buffer registers and flags

Flags	Register name	Bit	Register address
FIFOLength[6:0]	FIFOLength	6 to 0	04h
FIFOOvfl	ErrorFlag	4	0Ah
FlushFIFO	Control	0	09h
HiAlert	PrimaryStatus	1	03h
HiAlertIEn	InterruptEn	1	06h
HiAlertIRq	InterruptRq	1	07h
LoAlert	PrimaryStatus	0	03h
LoAlertIEn	InterruptEn	0	06h
LoAlertIRq	InterruptRq	0	07h
WaterLevel[5:0]	FIFOLevel	5 to 0	29h

8.4 Interrupt request system

The FSV9504 indicates interrupt events by setting the PrimaryStatus register bit IRq (see Section 9.5.1.4 “PrimaryStatus register” on page 41) and activating pin IRQ. The signal on pin IRQ can be used to interrupt the microprocessor using its interrupt handling capabilities ensuring efficient microprocessor software.

8.4.1 Interrupt sources overview

Table 14 shows the integrated interrupt flags, related source and setting condition. The interrupt TimerIRq flag bit indicates an interrupt set by the timer unit. Bit TimerIRq is set when the timer decrements from one down to zero (bit TAutoRestart disabled) or from one to the TReLoadValue[7:0] with bit TAutoRestart enabled.

Bit TxIRq indicates interrupts from different sources and is set as follows:

- the transmitter automatically sets the bit TxIRq interrupt when it is active and its state changes from sending data to transmitting the end of frame pattern
- the CRC coprocessor sets the bit TxIRq after all data from the FIFO buffer has been processed indicated by bit CRCReady = logic 1
- when EEPROM programming is finished, the bit TxIRq is set and is indicated by bit E2Ready = logic 1

The RxIRq flag bit indicates an interrupt when the end of the received data is detected. The IdleIRq flag bit is set when a command finishes and the content of the Command register changes to Idle.

When the FIFO buffer reaches the HIGH-level indicated by the WaterLevel[5:0] value (see Section 8.3.3 on page 13) and bit HiAlert = logic 1, then the HiAlertIRq flag bit is set to logic 1.

When the FIFO buffer reaches the LOW-level indicated by the WaterLevel[5:0] value (see Section 8.3.3 on page 13) and bit LoAlert = logic 1, then LoAlertIRq flag bit is set to logic 1.

Table 14. Interrupt sources

Interrupt flag	Interrupt source	Trigger action
TimerIRq	timer unit	timer counts from 1 to 0
TxIRq	transmitter	a data stream, transmitted to the label, ends
	CRC coprocessor	all data from the FIFO buffer has been processed
RxIRq	receiver	a data stream, received from the label, ends
IdleIRq	Command register	command execution finishes
HiAlertIRq	FIFO buffer	FIFO buffer is full
LoAlertIRq	FIFO buffer	FIFO buffer is empty

8.4.2 Interrupt request handling

8.4.2.1 Controlling interrupts and getting their status

The FSV9504 informs the microprocessor about the interrupt request source by setting the relevant bit in the InterruptRq register. The relevance of each interrupt request bit as source for an interrupt can be masked by the InterruptEn register interrupt enable bits.

Table 15. Interrupt control registers

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
InterruptEn	SetIEn	reserved	TimerIEn	TxIEn	RxIEn	IdleIEn	HiAlertIEn	LoAlertIEn
InterruptRq	SetIRq	reserved	TimerIRq	TxIRq	RxIRq	IdleIRq	HiAlertIRq	LoAlertIRq

If any interrupt request flag is set to logic 1 (showing that an interrupt request is pending) and the corresponding interrupt enable flag is set, the PrimaryStatus register IRq flag bit is set to logic 1. Different interrupt sources can activate simultaneously because all interrupt request bits are ORed, coupled to the IRq flag and then forwarded to pin IRQ.

8.4.2.2 Accessing the interrupt registers

The interrupt request bits are automatically set by the FSV9504's internal state machines. In addition, the microprocessor can also set or clear the interrupt request bits as required.

A special implementation of the InterruptRq and InterruptEn registers enables changing an individual bit status without influencing any other bits. If an interrupt register is set to logic 1, bit SetIxx and the specific bit must both be set to logic 1 at the same time. Vice versa, if a specific interrupt flag is cleared, zero must be written to the SetIxx and the interrupt register address must be set to logic 1 at the same time.

If a content bit is not changed during the setting or clearing phase, zero must be written to the specific bit location.

Example: Writing 3Fh to the InterruptRq register clears all bits. SetIRq is set to logic 0 while all other bits are set to logic 1. Writing 81h to the InterruptRq register sets LoAlertIRq to logic 1 and leaves all other bits unchanged.

8.4.3 Configuration of pin IRQ

The logic level of the IRq flag bit is visible on pin IRQ. The signal on pin IRQ can also be controlled using the following IRQPinConfig register bits.

- bit IRQInv: the signal on pin IRQ is equal to the logic level of bit IRq when this bit is set to logic 0. When set to logic 1, the signal on pin IRQ is inverted with respect to bit IRq.

- bit IRQPushPull: when set to logic 1, pin IRQ has CMOS output characteristics. When it is set to logic 0, it is an open-drain output which requires an external resistor to achieve a HIGH-level at pin IRQ.

Remark: During the reset phase (see Section 8.7.2 on page 23) bit IRQInv is set to logic 1 and bit IRQPushPull is set to logic 0. This results in a high-impedance on pin IRQ.

8.4.4 Register overview interrupt request system

Table 16 shows the related interrupt request system flags in alphabetical order.

Table 16. Associated Interrupt request system registers and flags

Flags	Register name	Bit	Register address
HiAlertIEn	InterruptEn	1	06h
HiAlertIRq	InterruptRq	1	07h
IdleIEn	InterruptEn	2	06h
IdleIRq	InterruptRq	2	07h
IRq	PrimaryStatus	3	03h
IRQInv	IRQPinConfig	1	07h
IRQPushPull	IRQPinConfig	0	07h
LoAlertIEn	InterruptEn	0	06h
LoAlertIRq	InterruptRq	0	07h
RxIEn	InterruptEn	3	06h
RxIRq	InterruptRq	3	07h
SetIEn	InterruptEn	7	06h
SetIRq	InterruptRq	7	07h
TimerIEn	InterruptEn	5	06h
TimerIRq	InterruptRq	5	07h
TxIEn	InterruptEn	4	06h
TxIRq	InterruptRq	4	07h

8.5 Timer unit

The timer derives its clock from the 13.56 MHz on-board chip clock. The microprocessor can use this timer to manage timing-relevant tasks.

The timer unit may be used in one of the following configurations:

- Timeout counter
- WatchDog counter
- Stopwatch
- Programmable one shot
- Periodical trigger

The timer unit can be used to measure the time interval between two events or to indicate that a specific timed event occurred. The timer is triggered by events but does not influence any event (e.g. a time-out during data receiving does not automatically influence the receiving process). Several timer related flags can be set and these flags can be used to generate an interrupt.

8.5.1 Timer unit implementation

8.5.1.1 Timer unit block diagram

Figure 6 shows the block diagram of the timer module.

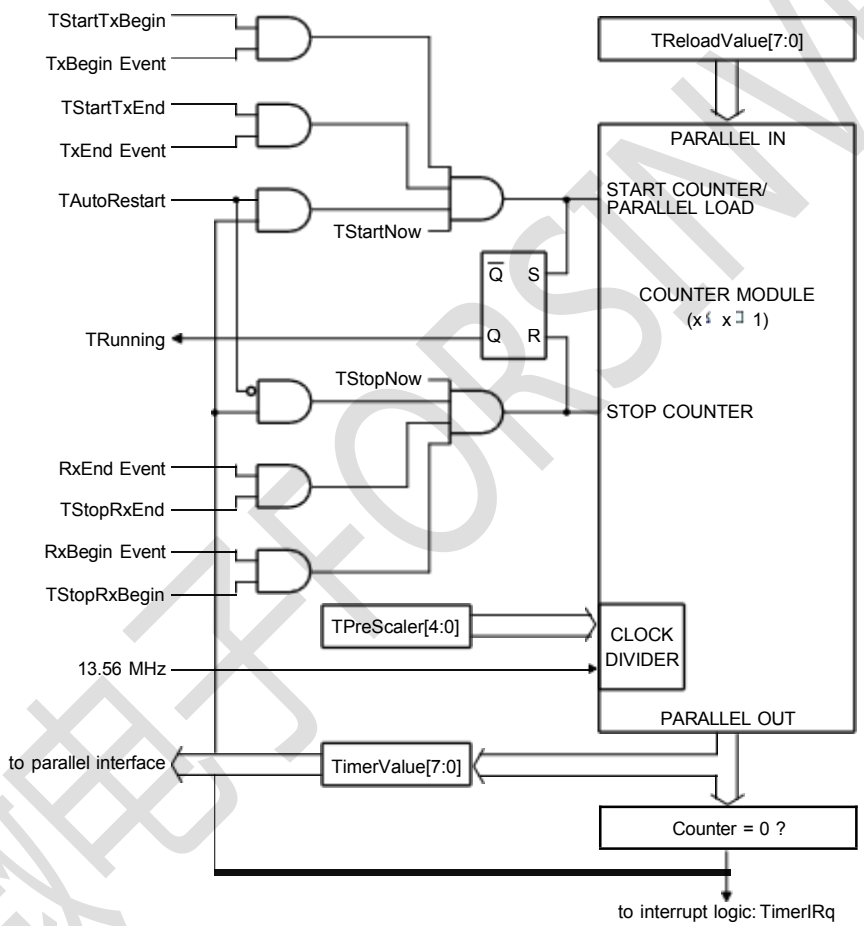


Fig 6. Timer module block diagram

The timer unit is designed, so that events when combined with enabling flags start or stop the counter. For example, setting bit TStartTxBegin = logic 1 enables control of received data with the timer unit. In addition, the first received bit is indicated by the TxBegin event. This combination starts the counter at the defined TReloadValue[7:0].

The timer stops automatically when the counter value is equal to zero or if a defined stop event happens (TautoRestart not enabled).

8.5.1.2 Controlling the timer unit

The main part of the timer unit is a down-counter. As long as the down-counter value is not zero, it decrements its value with each timer clock cycle.

If the TAutoRestart flag is enabled, the timer does not decrement down to zero. On reaching value 1, the timer reloads the next clock function with the TReloadValue[7:0].

The timer is started immediately by loading a value from the TimerReload register into the counter module.

This is activated by one of the following events:

- transmission of the first bit to the label (TxBegin event) with bit TStartTxBegin = logic 1
- transmission of the last bit to the label (TxEnd event) with bit TStartTxEnd = logic 1
- bit TStartNow is set to logic 1 by the microprocessor

Remark: Every start event reloads the timer from the TimerReload register. Thus, the timer unit is re-triggered.

The timer can be configured to stop on one of the following events:

- receipt of the first valid bit from the label (RxBegin event) with bit TStopRxBegin = logic 1
- receipt of the last bit from the label (RxEnd event) with bit TStopRxEnd = logic 1
- the counter module has decremented down to zero and bit TAutoRestart = logic 0
- bit TStopNow is set to logic 1 by the microprocessor.

Loading a new value, e.g. zero, into the TimerReload register or changing the timer unit while it is counting will not immediately influence the counter. In both cases, this is because this register only affects the counter content after a start event. Thus, the TimerReload register may be changed even if the timer unit is already counting. The consequence of changing the TimerReload register will be visible after the next start event.

If the counter is stopped when bit TStopNow is set, no TimerIRq is flagged.

8.5.1.3 Timer unit clock and period

The timer unit clock is derived from the 13.56 MHz on-board chip clock using the programmable divider. Clock selection is made using the TimerClock register TPreScaler[4:0] bits based on Equation 3:

$$f_{TimerClock} \quad \frac{1}{T_{TimerClock}} \quad \frac{2^{TPreScaler}}{13.56} = [MHz]$$

The values for the TPreScaler[4:0] bits are between 0 and 21 which results in a minimum periodic time ($T_{TimerClock}$) of between 74 ns and 150 ms.

The time period elapsed since the last start event is calculated using Equation 4:

$$t_{Timer} = \frac{TReLoadValue - TimerValue}{f_{TimerClock}} \quad [s]$$

This results in a minimum time period (t_{Timer}) of between 74 ns and 40 s.

8.5.1.4 Timer unit status

The SecondaryStatus register's TRunning bit shows the timer's status. Configured start events start the timer at the TReloadValue[7:0] and changes the status flag TRunning to logic 1. Conversely, configured stop events stop the timer and sets the TRunning status flag to logic 0. As long as status flag TRunning is set to logic 1, the TimerValue register changes on the next timer unit clock cycle.

The TimerValue[7:0] bits can be read directly from the TimerValue register.

8.5.1.5 Time-slot period

When sending ICODE1 Quit frames, it is necessary to generate the exact chronological relationship to the start of the command frame.

If at the end of command execution TimeSlotPeriod > 0, the TimeSlotPeriod starts. If the FIFO buffer contains data when the end of TimeSlotPeriod is reached, the data is sent. If the FIFO buffer is empty nothing happens. As long as the TimeSlotPeriod is > 0, the TimeSlotPeriod counter automatically starts on reaching the end.

This forms the exact time relationship between the start and finish of the command frame used to generate and send ICODE1 Quit frames.

When the TimeSlotPeriod > 0, the next Frame starts with exactly the same interval TimeSlotPeriod/CoderRate delayed after each previous send frame. CoderRate defines the clock frequency of the encoder. If TimeSlotPeriod[7:0] = 0, the send function is not automatically triggered.

The content of the TimeSlotPeriod register can be changed while it is running but the change is only effective after the next TimeSlotPeriod restart.

Example:

- CoderRate = 0 × 0.5 (~52.97 kHz)
- The interval should be 8.458 ms for ICODE1 standard mode

TimeSlotPeriod = CoderRate × Interval = 52.97 kHz × 8.458 ms □1 = 447 = 1BFh

Remark: The TimeSlotPeriod MSB bit is contained in the SIGOUTSelect register.

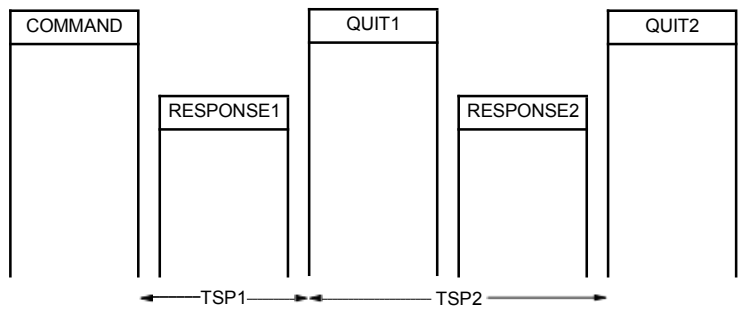


Fig 7. TimeSlotPeriod

Table 17. TimeSlotPeriod

ICODE1 mode	TimeSlotPeriod for TSP1	TimeSlotPeriod for TSP2
standard mode	BFh	1BFh
fast mode	5Fh	67h

Remark: Set bit TxCRCEn to logic 0 before the Quit frame is sent. If TxCRCEn is not set to logic 0, the Quit frame is sent with a calculated CRC value. Use the CRC8 algorithm to calculate the Quit value.

8.5.2 Using the timer unit functions

8.5.2.1 Time-out and WatchDog counters

After starting the timer using TReloadValue[7:0], the timer unit decrements the TimerValue register beginning with a given start event. If a given stop event occurs, such as a bit being received from the label, the timer unit stops without generating an interrupt.

If a stop event does not occur, such as the label not answering within the expected time, the timer unit decrements down to zero and generates a timer interrupt request. This signals to the microprocessor the expected event has not occurred within the given time (t_{Timer}).

8.5.2.2 Stopwatch

The time (t_{Timer}) between a start and stop event is measured by the microprocessor using the timer unit. Setting the TimerReload register triggers the timer which in turn, starts to decrement. If the defined stop event occurs, the timer stops. The time between start and stop is calculated by the microprocessor using Equation 5, when the timer does not decrement down to zero.

$$\Delta t = TReLoad_{value} - TimerValue \times t_{Timer}$$

8.5.2.3 Programmable one shot timer and periodic trigger

Programmable one shot timer: The microprocessor starts the timer unit and waits for the timer interrupt. The interrupt occurs after the time specified by t_{Timer} (TAutoRestart bit = logic 0).

Periodic trigger: If the microprocessor sets the TAutoRestart bit, and TReloadValue is not equal to zero, it generates an interrupt request after every t_{Timer} cycle.

8.5.3 Timer unit registers

Table 18 shows the related flags of the timer unit in alphabetical order.

Table 18. Associated timer unit registers and flags

Flags	Register name	Bit	Register address
TAutoRestart	TimerClock	5	2Ah
TimerValue[7:0]	TimerValue	7 to 0	0Ch
TReloadValue[7:0]	TimerReload	7 to 0	2Ch
TPreScaler[4:0]	TimerClock	4 to 0	2Ah
TRunning	SecondaryStatus	7	05h
TStartNow	Control	1	09h

Table 18. Associated timer unit registers and flags

Flags	Register name	Bit	Register address
TStartTxBegin	TimerControl	0	2Bh
TStartTxEnd	TimerControl	1	2Bh
TStopNow	Control	2	09h
TStopRxBegin	TimerControl	2	2Bh
TStopRxEnd	TimerControl	3	2Bh

8.6 Power reduction modes

8.6.1 Hard power-down

Hard power-down is enabled when pin RSTPD is HIGH. This turns off all internal current sinks including the oscillator. All digital input buffers are separated from the input pads and defined internally (except pin RSTPD itself). The output pins are frozen at a given value. The status of all pins during a hard power-down is shown in Table 19.

Table 19. Signal on pins during Hard power-down

Symbol	Pin	Type	Description
OSCIN	1	I	not separated from input, pulled to AVSS
IRQ	2	O	high-impedance
n.c.	3	I	separated from input
SIGOUT	4	O	LOW
TX1	5	O	HIGH
TX2	7	O	LOW
NCS	9	I	separated from input
NWR	10	I	separated from input
NRD	11	I	separated from input
D0 to D7	13 to 20	I/O	separated from input
ALE	21	I	separated from input
A0	22	I/O	separated from input
A1	23	I	separated from input
A2	24	I	separated from input
AUX	27	O	high-impedance
RX	29	I	not changed
VMID	30	A	pulled to V_{DDA}
RSTPD	31	I	not changed
OSCOUT	32	O	HIGH

8.6.2 Soft power-down mode

Soft power-down mode is entered immediately using the Control register bit PowerDown.

All internal current sinks, including the oscillator buffer, are switched off. The digital input buffers are not separated from the input pads and keep their functionality. In addition, the digital output pins do not change their state.

After resetting the Control register bit PowerDown, the bit indicating Soft power-down mode is only cleared after 512 clock cycles. Resetting it does not immediately clear it. The PowerDown bit is automatically cleared when the Soft power-down mode is exited.

Remark: When the internal oscillator is used, time (t_{osc}) is required for the oscillator to become stable. This is because the internal oscillator is supplied by V_{DDA} and any clock cycles will not be detected by the internal logic until V_{DDA} is stable.

8.6.3 Standby mode

The Standby mode is immediately entered when the Control register StandBy bit is set. All internal current sinks, including the internal digital clock buffer are switched off. However, the oscillator buffer is not switched off.

The digital input buffers are not separated by the input pads, keeping their functionality and the digital output pins do not change their state. In addition, the oscillator does not need time to wake-up.

After resetting the Control register StandBy bit, it takes four clock cycles on pin OSCIN for Standby mode to exit. Resetting bit StandBy does not immediately clear it. It is automatically cleared when the Standby mode is exited.

8.6.4 Automatic receiver power-down

It is a power saving feature to switch off the receiver circuit when it is not needed. Setting bit RxAutoPD = logic 1, automatically powers down the receiver when it is not in use. Setting bit RxAutoPD = logic 0, keeps the receiver continuously powered up.

8.7 StartUp phase

The events executed during the StartUp phase are shown in Figure 8.

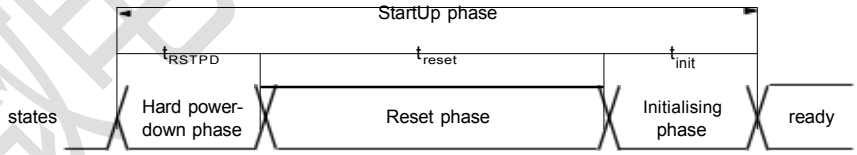


Fig 8. The StartUp procedure

8.7.1 Hard power-down phase

The hard power-down phase is active during the following cases:

- a Power-On Reset (POR) caused by power-up on pins DVDD activated when V_{DDD} is below the digital reset threshold.
- a Power-On Reset (POR) caused by power-up on pins AVDD activated when V_{DDA} is below the analog reset threshold.
- a HIGH-level on pin RSTPD which is active while pin RSTPD is HIGH. The HIGH level period on pin RSTPD must be at least 100 µs ($t_{PD} \geq 100$ µs). Shorter phases will not necessarily result in the reset phase (t_{reset}). The rising or falling edge slew rate on pin RSTPD is not critical because pin RSTPD is a Schmitt trigger input.

8.7.2 Reset phase

The reset phase automatically follows the Hard power-down. Once the oscillator is running stably, the reset phase takes 512 clock cycles. During the reset phase, some register bits are preset by hardware. The respective reset values are given in the description of each register (see Section 9.5 on page 40).

Remark: When the internal oscillator is used, time (t_{osc}) is required for the oscillator to become stable. This is because the internal oscillator is supplied by V_{DDA} and any clock cycles will not be detected by the internal logic until V_{DDA} is stable.

8.7.3 Initialization phase

The initialization phase automatically follows the reset phase and takes 128 clock cycles. During the initializing phase the content of the EEPROM blocks 1 and 2 is copied into the register subaddresses 10h to 2Fh (see Section 8.2.2 on page 10).

Remark: During the production test, the FSV9504 is initialized with default configuration values. This reduces the microprocessor's configuration time to a minimum.

8.7.4 Initializing the parallel interface type

A different initialization sequence is used for each microprocessor. This enables detection of the correct microprocessor interface type and synchronization of the microprocessor's and the FSV9504's start-up. See Section 8.1.3 on page 7 for detailed information on the different connections for each microprocessor interface type.

During StartUp phase, the command value is set to 3Fh once the oscillator attains clock frequency stability at an amplitude of > 90 % of the nominal 13.56 MHz clock frequency. At the end of the initialization phase, the FSV9504 automatically switches to idle and the command value changes to 00h.

To ensure correct detection of the microprocessor interface, the following sequence is executed:

- the Command register is read until the 6-bit register value is 00h. On reading the 00h value, the internal initialization phase is complete and the FSV9504 is ready to be controlled
- write 80h to the Page register to initialize the microprocessor interface
- read the Command register. If it returns a value of 00h, the microprocessor interface was successfully initialized
- write 00h to the Page registers to activate linear addressing mode.

8.8 Oscillator circuit

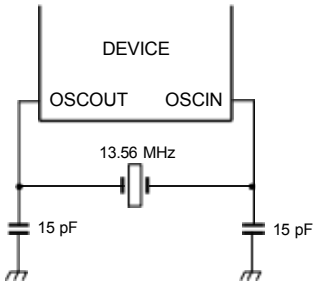


Fig 9. Quartz clock connection

The clock applied to the FSV9504 acts as a time basis for the synchronous system encoder and decoder. The stability of the clock frequency is an important factor for correct operation. To obtain highest performance, clock jitter must be as small as possible. This is best achieved by using the internal oscillator buffer with the recommended circuitry.

If an external clock source is used, the clock signal must be applied to pin OSCIN. In this case, be very careful in optimizing clock duty cycle and clock jitter. Ensure the clock quality has been verified. It must meet the specifications described in Section 12.4.4 on page 84.

Remark: We do not recommend using an external clock source.

8.9 Transmitter pins TX1 and TX2

The signal on pins TX1 and TX2 is the 13.56 MHz carrier modulated by an envelope signal. It can be used to drive an antenna directly, using minimal passive components for matching and filtering (see Section 14.1 on page 85). To enable this, the output circuitry is designed with a very low-impedance source resistance. The TxControl register is used to control the TX1 and TX2 signals.

8.9.1 Configuring pins TX1 and TX2

TX1 pin configurations are described in Table 20.

Table 20. Pin TX1 configurations

TxControl register configuration	Envelope	TX1 signal
TX1RFEn		
0	X	LOW (GND)
1	0	13.56 MHz modulated carrier
1	1	13.56 MHz unmodulated carrier

TX2 pin configurations are described in Table 21.

Table 21. Pin TX2 configurations

TxControl register configuration			Envelope	TX2 signal
TX2RFEn	TX2Cw	TX2Inv		
0	X	X	X	LOW (GND)
1	0	0	0	13.56 MHz modulated carrier
1	0	0	1	13.56 MHz unmodulated carrier
1	0	1	0	13.56 MHz modulated carrier frequency, 180° phase-shift relative to TX1
1	0	1	1	13.56 MHz unmodulated carrier, 180° phase-shift relative to TX1
1	1	0	X	13.56 MHz unmodulated carrier
1	1	1	X	13.56 MHz unmodulated carrier, 180° phase-shift relative to TX1

8.9.2 Antenna operating distance versus power consumption

Using different antenna matching circuits (by varying the supply voltage on the antenna driver supply pin TVDD), it is possible to find the trade-off between maximum effective operating distance and power consumption. Different antenna matching circuits are described in the Application note Ref. 1.

8.9.3 Antenna driver output source resistance

The output source conductance of pins TX1 and TX2 for driving a HIGH level can be adjusted between 1 Ω and 100 Ω using the CwConductance register GsCfgCW[5:0] bits.

The values are relative to the reference source resistance ($R_{S(ref)}$) which is measured during the production test and stored in the FSV9504 EEPROM. It can be read from the product information field (see Section 8.2.1 on page 9). The electrical specification can be found in Section 12.3.3 on page 79.

8.9.3.1 Source resistance table

Table 22. TX1 and TX2 source resistance of n-channel driver transistor against GsCfgCW
MANT = Mantissa; EXP = Exponent.

GsCfgCW (decimal)	$EXP_{GsCfgCW}$ (decimal)	$MANT_{GsCfgCW}$ (decimal)	$R_{S(ref)}$ (Ω)	GsCfgCW (decimal)	$EXP_{GsCfgCW}$ (decimal)	$MANT_{GsCfgCW}$ (decimal)	$R_{S(ref)}$ (Ω)
0	0	0	∞	24	1	8	0.0652
16	1	0	∞	25	1	9	0.0580
32	2	0	∞	37	2	5	0.0541
48	3	0	∞	26	1	10	0.0522
1	0	1	1.0000	27	1	11	0.0474
17	1	1	0.5217	51	3	3	0.0467
2	0	2	0.5000	38	2	6	0.0450
3	0	3	0.3333	28	1	12	0.0435
33	2	1	0.2703	29	1	13	0.0401
18	1	2	0.2609	39	2	7	0.0386
4	0	4	0.2500	30	1	14	0.0373
5	0	5	0.2000	52	3	4	0.0350
19	1	3	0.1739	31	1	15	0.0348
6	0	6	0.1667	40	2	8	0.0338
7	0	7	0.1429	41	2	9	0.0300
49	3	1	0.1402	53	3	5	0.0280
34	2	2	0.1351	42	2	10	0.0270
20	1	4	0.1304	43	2	11	0.0246
8	0	8	0.1250	54	3	6	0.0234
9	0	9	0.1111	44	2	12	0.0225
21	1	5	0.1043	45	2	13	0.0208
10	0	10	0.1000	55	3	7	0.0200
11	0	11	0.0909	46	2	14	0.0193
35	2	3	0.0901	47	2	15	0.0180
22	1	6	0.0870	56	3	8	0.0175
12	0	12	0.0833	57	3	9	0.0156
13	0	13	0.0769	58	3	10	0.0140
23	1	7	0.0745	59	3	11	0.0127
14	0	14	0.0714	60	3	12	0.0117
50	3	2	0.0701	61	3	13	0.0108
36	2	4	0.0676	62	3	14	0.0100
15	0	15	0.0667	63	3	15	0.0093

8.9.3.2 Changing the modulation index

Table Table 23 shows the modulation index values when using an antenna with a resistance (R_{ant}) of 50 Ω with ModConductance register's GsCfgMod[5:0] values between 00h and 3Fh. Note that if the modulation index value is changed the GsCfgMod[5:0] value must also be changed.

Table 23. Modulation index values

GsCfgMod[5:0] (Hex)	Relative resistance during modulation (Ω)	Modulation index (R_{ant} = 50 Ω) (%)	GsCfgMod[5:0] (Hex)	Relative resistance during modulation (Ω)	Modulation index (R_{ant} = 50 Ω) (%)
00	∝	-	18	0.065	4.15
10	∝	-	19	0.058	3.63
20	∝	-	25	0.054	3.35
30	∝	-	1A	0.052	3.22
01	1	43.45	1B	0.047	2.87
11	0.522	28.44	33	0.047	2.82
02	0.5	27.57	26	0.045	2.69
03	0.333	20.08	1C	0.043	2.58
21	0.27	16.83	1D	0.040	2.33
12	0.261	16.33	27	0.039	2.22
04	0.25	15.73	1E	0.037	2.12
05	0.2	12.88	34	0.035	1.95
13	0.174	11.32	1F	0.035	1.93
06	0.167	10.88	28	0.034	1.86
07	0.143	9.38	29	0.030	1.58
31	0.14	9.21	35	0.028	1.43
22	0.135	8.89	2A	0.027	1.35
14	0.13	8.59	2B	0.025	1.17
08	0.125	8.23	36	0.023	1.08
09	0.111	7.32	2C	0.023	1.01
15	0.104	6.86	2D	0.021	0.88
0A	0.1	6.57	37	0.02	0.82
0B	0.091	5.95	2E	0.019	0.77
23	0.090	5.89	2F	0.018	0.67
16	0.087	5.68	38	0.018	0.63
0C	0.083	5.43	39	0.016	0.48
0D	0.077	4.98	3A	0.014	0.36
17	0.075	4.81	3B	0.013	0.26
0E	0.071	4.59	3C	0.012	0.18
32	0.070	4.5	3D	0.011	0.11
24	0.068	4.32	3E	0.01	0.05
0F	0.067	4.26	3F	0.009	0

8.9.3.3 Calculating the relative source resistance

The reference source resistance $R_{S(ref)}$ can be calculated using Equation 6.

$$R_{S\,ref(\ )} = \frac{1}{MANT_{GsCfgCW} \cdot \left(\frac{77}{40}\right)^{EXP_{GsCfgCW}}}$$

8.9.3.4 Calculating the effective source resistance

Wiring resistance ($R_{S(wire)}$): Wiring and bonding add a constant offset to the driver resistance that is relevant when pins TX1 and TX2 are switched to low-impedance. The additional resistance for pin TX1 ($R_{S(wire)TX1}$) can be set approximately as shown in Equation 7.

$$R_{S\,wir(\ TX1)} \approx 500\ m\Omega$$

Effective resistance (R_{Sx}): The source resistances of the driver transistors (RsMaxP byte) read from the Product Information Field (see Section 8.2.1 on page 9) are measured during the production test with CwConductance register's GsCfgCW[5:0] = 01h.

To calculate the driver resistance for a specific value set in ModConductance register 's GsCfgMod[5:0], use Equation 8.

$$R_{Sx} = R_{S\,ref(\ )max(P} R_{S\,wir(\ TX1)} \cdot R_{S\,re(\ )+)} R_{S\,wir(\ TX1)}$$

8.9.4 Pulse width

The envelope carries the data signal information that is transmitted to the label. The data signal is encoded using either 1 out of 256 RZ, or 1 out of 4 codes. In addition, each pause of the encoded signal is again encoded as a pulse of a certain width. The width of the pulse is adjusted using the ModWidth register. The pulse width (t_w) is calculated using Equation 9 where the clock frequency constant (f_{clk}) = 13.56 MHz.

$$t_w = 2\frac{ModWidth + 1}{f_{clk}}$$

8.10 Receiver circuitry

The FSV9504 uses an integrated quadrature demodulation circuit which extracts the subcarrier signal from the 13.56 MHz ASK-modulated signal on pin RX.

The quadrature demodulator uses two different clocks (Q-clock and I-clock) with a phase-shift of 90° between them. Both resulting subcarrier signals are amplified, filtered and forwarded to the correlation circuitry. The correlation results are evaluated, digitized and then passed to the digital circuitry. Various adjustments can be made to obtain optimum performance for all processing units.

8.10.1 Receiver circuit block diagram

Figure 10 shows the block diagram of the receiver circuit. The receiving process can be broken down in to several steps. Quadrature demodulation of the 13.56 MHz carrier signal is performed. To achieve the optimum performance, automatic Q-clock calibration is recommended (see Section 8.10.2.1 on page 29).

The demodulated signal is amplified by an adjustable amplifier. A correlation circuit calculates the degree of similarity between the expected and the received signal. The BitPhase register enables correlation interval position alignment with the received signal's bit grid. In the evaluation and digitizer circuitry, the valid bits are detected and the digital results are sent to the FIFO buffer. Several tuning steps are possible for this circuit.

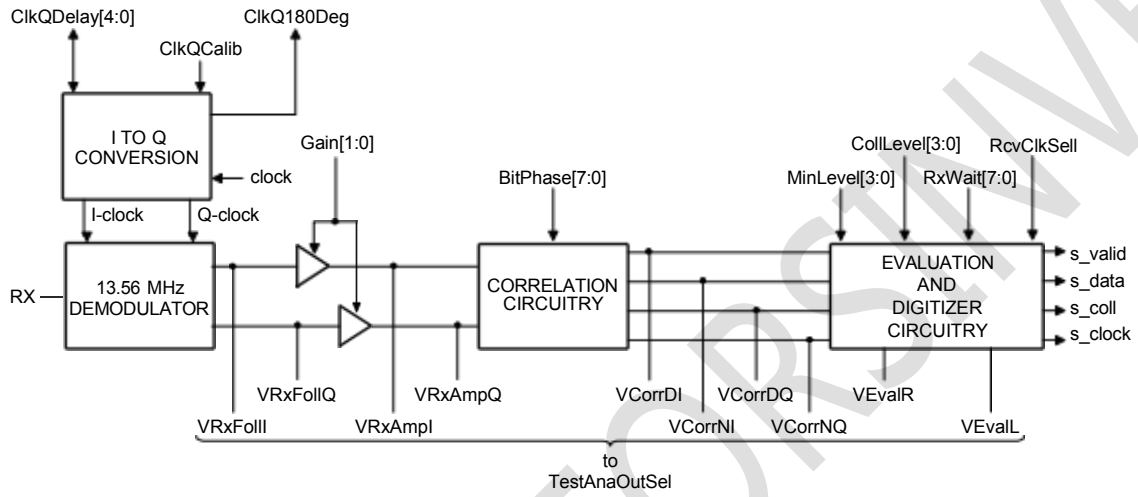


Fig 10. Receiver circuit block diagram

The signal can be observed on its way through the receiver as shown in Figure 10. One signal at a time can be routed to pin AUX using the TestAnaSelect register as described in Section 14.2.2 on page 88.

8.10.2 Receiver operation

In general, the default settings programmed in the StartUp initialization file are suitable for use with the FSV9504 to ICODE label data communication. However, in some environments specific user settings will achieve better performance.

8.10.2.1 Automatic Q-clock calibration

The quadrature demodulation concept of the receiver generates a phase signal (I-clock) and a 90° phase-shifted quadrature signal (Q-clock). To achieve the optimum demodulator performance, the Q-clock and the I-clock must be phase-shifted by 90°. After the reset phase, a calibration procedure is automatically performed.

Automatic calibration can be set-up to execute at the end of each Transceive command if bit ClkQCalib = logic 0. Setting bit ClkQCalib = logic 1 disables all automatic calibrations except after the reset sequence. Automatic calibration can also be triggered by the software when bit ClkQCalib has a logic 0 to logic 1 transition.

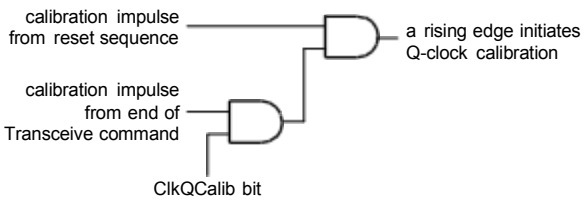


Fig 11. Automatic Q-clock calibration

Remark: The duration of the automatic Q-clock calibration is 65 oscillator periods or approximately 4.8 µs.

The ClockQControl register's ClkQDelay[4:0] value is proportional to the phase-shift between the Q-clock and the I-clock. The ClkQ180Deg status flag bit is set when the phase-shift between the Q-clock and the I-clock is greater than 180°.

Remark:

- The StartUp initialization file enables automatic Q-clock calibration after a reset
- If bit ClkQCalib = logic 1, automatic calibration is not performed. Leaving this bit set to logic 1 can be used to permanently disable automatic calibration.
- It is possible to write data to the ClkQDelay[4:0] bits using the microprocessor. The aim could be to disable automatic calibration and set the delay using the software. Configuring the delay value using the software requires bit ClkQCalib to have been previously set to logic 1 and a time interval of at least 4.8 µs has elapsed. Each delay value must be written with bit ClkQCalib set to logic 1. If bit ClkQCalib is logic 0, the configured delay value is overwritten by the next automatic calibration interval.

8.10.2.2 Amplifier

The demodulated signal must be amplified by the variable amplifier to achieve the best performance. The gain of the amplifiers can be adjusted using the RxControl1 register Gain[1:0] bits; see Table 24.

Table 24. Gain factors for the internal amplifier
See Table 77 "RxControl1 register bit descriptions" on page 52 for additional information.

Register setting	Gain factor (simulation results)	Gain factor [dB] (simulation results)
00	22	20
01	35	24
10	82	31
11	130	35

8.10.2.3 Correlation circuitry

The correlation circuitry calculates the degree of matching between the received and an expected signal. The output is a measure of the amplitude of the expected signal in the received signal. This is done for both, the Q and I-channels. The correlator provides two outputs for each of the two input channels, resulting in a total of four output signals.

The correlation circuitry needs the phase information for the incoming label signal for optimum performance. This information is defined for the microprocessor using the BitPhase register. This value defines the phase relationship between the transmitter and receiver clock in multiples of the BitPhase time ($t_{BitPhase}$) = 1 / 13.56 MHz.

8.10.2.4 Evaluation and digitizer circuitry

The correlation results are evaluated for each bit-half of the Manchester coded signal. The evaluation and digitizer circuit decides from the signal strengths of both bit-halves, if the current bit is valid

- If the bit is valid, its value is identified
- If the bit is not valid, it is checked to identify if it contains a bit-collision

Select the following levels for optimal using RxThreshold register bits:

- **MinLevel[3:0]:** defines the minimum signal strength of the stronger bit-halve's signal which is considered valid.
- **CollLevel[3:0]:** defines the minimum signal strength relative to the amplitude of the stronger half-bit that has to be exceeded by the weaker half-bit of the Manchester coded signal to generate a bit-collision. If the signal's strength is below this value, logic 1 and logic 0 can be determined unequivocally.

After data transmission, the label is not allowed to send its response before a preset time period which is called the frame guard time in the ISO/IEC 15693 standard (similar to ICODE1). The length of this time period is set using the RxWait register's RxWait[7:0] bits. The RxWait register defines when the receiver is switched on after data transmission to the label in multiples of one bit duration.

If bit RcvClkSell is set to logic 1, the I-clock is used to clock the correlator and evaluation circuits. If bit RcvClkSell is set to logic 0, the Q-clock is used.

Remark: It is recommended to use the Q-clock.

8.11 Serial signal switch

The FSV9504 comprises two main blocks:

- **digital circuitry:** comprising the state machines, encoder and decoder logic etc.
- **analog circuitry**: comprising the modulator, antenna drivers, receiver and amplification circuitry

The interface between these two blocks can be configured so that the interface signals are routed to pin SIGOUT.

8.11.1 Serial signal switch block diagram

Figure 12 shows the serial signal switches. Three different switches are implemented in the serial signal switch enabling the FSV9504 to be used in different configurations.

The serial signal switch can also be used to check the transmitted and received data during the design-in phase or for test purposes. Section 14.2.1 on page 87 describes the analog test signals and measurements at the serial signal switch.

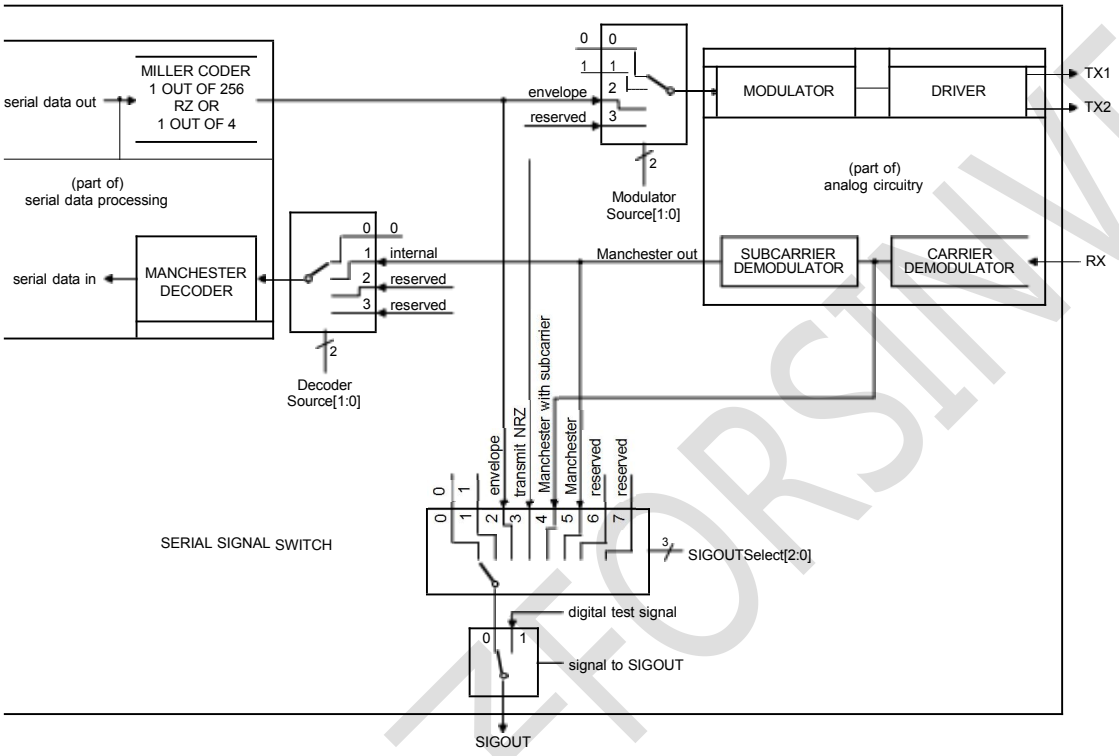


Fig 12. Serial signal switch block diagram

Section 8.11.2 describes the relevant registers and settings used to configure and control the serial signal switch.

8.11.2 Serial signal switch registers

The RxControl2 register DecoderSource[1:0] bits define the input signal for the internal Manchester decoder and are described in Table 25.

Table 25. DecoderSource[1:0] values

See Table 86 on page 54 for additional information.

Number	DecoderSource [1:0]	Input signal to decoder
0	00	constant 0
1	01	output of the analog part. This is the default configuration
2	10	reserved
3	11	reserved

The TxControl register ModulatorSource[1:0] bits define the signal used to modulate the transmitted 13.56 MHz carrier frequency. The modulated signal drives pins TX1 and TX2.

Table 26. ModulatorSource[1:0] values
See Table 86 on page 54 for additional information.

Number	ModulatorSource [1:0]	Input signal to modulator
0	00	constant 0 (carrier signal off on pins TX1 and TX2)
1	01	constant 1 (continuous carrier signal on pins TX1 and TX2)
2	10	modulation signal (envelope) from the internal encoder. This is the default configuration.
3	11	reserved

The SIGOUTSelect register's SIGOUTSelect[2:0] bits select the input signal to be routed to the internal Manchester decoder.

Table 27. SIGOUTSelect[2:0] values
See Table 100 on page 57 for additional information.

Number	SIGOUTSelect [2:0]	Signal routed to pin SIGOUT
0	000	constant LOW
1	001	constant HIGH
2	010	modulation signal (envelope) from the internal encoder
3	011	serial data stream to be transmitted; the same as for SIGOUTSelect[2:0] = 001 but not encoded by the selected pulse encoder
4	100	output signal of the receiver circuit; label modulation signal regenerated and delayed
5	101	output signal of the subcarrier demodulator; Manchester coded label signal
6	110	reserved
7	111	reserved

Remark: To use the SIGOUTSelect[2:0] bits, the TestDigiSelect register SignalToSIGOUT bit must be logic 0.

9. FSV9504 registers

9.1 Register addressing modes

Three methods can be used to operate the FSV9504:

- initiating functions and controlling data by executing commands
- configuring the functional operation using a set of configuration bits
- monitoring the state of the FSV9504 by reading status flags

The commands, configuration bits and flags are accessed using the microprocessor interface. The FSV9504 can internally address 64 registers using six address lines.

9.1.1 Page registers

The FSV9504 register set is segmented into eight pages containing eight registers each. A Page register can always be addressed, irrespective of which page is currently selected.

9.1.2 Dedicated address bus

When using the FSV9504 with the dedicated address bus, the microprocessor defines three address lines using address pins A0, A1 and A2. This enables addressing within a page. To switch between registers in different pages a paging mechanism needs to be used.

Table 28 shows how the register address is assembled.

Table 28. Dedicated address bus: assembling the register address

Register bit: UsePageSelect	Register address					
1	PageSelect2	PageSelect1	PageSelect0	A2	A1	A0

9.1.3 Multiplexed address bus

The microprocessor may define all six address lines at once using the FSV9504 with a multiplexed address bus. In this case either the paging mechanism or linear addressing can be used.

Table 29 shows how the register address is assembled.

Table 29. Multiplexed address bus: assembling the register address

Multiplexed address bus type	UsePage Select	Register address					
Paging mode	1	PageSelect2	PageSelect1	PageSelect0	AD2	AD1	AD0
Linear addressing	0	AD5	AD4	AD3	AD2	AD1	AD0

9.2 Register bit behavior

Bits and flags for different registers behave differently, depending on their functions. In principle, bits with same behavior are grouped in common registers. Table 30 describes the function of the Access column in the register tables.

Table 30. Behavior and designation of register bits

Abbreviation	Behavior	Description
R/W	read and write	These bits can be read and written by the microprocessor. Since they are only used for control, their content is not influenced by internal state machines. **Example:** TimerReload register may be read and written by the microprocessor. It will also be read by internal state machines but never changed by them.
D	dynamic	These bits can be read and written by the microprocessor. Nevertheless, they may also be written automatically by internal state machines. **Example:** the Command register changes its value automatically after the execution of the command.
R	read only	These registers hold flags which have a value determined by internal states only. **Example:** the ErrorFlag register cannot be written externally but shows internal states.
W	write only	These registers are used for control only. They may be written by the microprocessor but cannot be read. Reading these registers returns an undefined value. **Example:** The TestAnaSelect register is used to determine the signal on pin AUX however, it is not possible to read its content.
0, 1 or X	generic value	Where applicable, the values 0 and 1 indicate the **expected** logic value for a given bit. Where X is used, any logic value can be entered.

9.3 Register overview

Table 31. FSV9504 register overview

Sub address (Hex)	Register name	Function	Refer to
Page 0: Command and status			
00h	Page	selects the page register	Table 33 on page 40
01h	Command	starts and stops command execution	Table 35 on page 40
02h	FIFOData	input and output of 64-byte FIFO buffer	Table 37 on page 41
03h	PrimaryStatus	receiver and transmitter and FIFO buffer status flags	Table 39 on page 41
04h	FIFOLength	number of bytes buffered in the FIFO buffer	Table 41 on page 42
05h	SecondaryStatus	secondary status flags	Table 43 on page 43
06h	InterruptEn	enable and disable interrupt request control bits	Table 45 on page 43
07h	InterruptRq	interrupt request flags	Table 47 on page 44
Page 1: Control and status			
08h	Page	selects the page register	Table 33 on page 40
09h	Control	control flags for functions such as timer and power saving	Table 49 on page 45
0Ah	ErrorFlag	show the error status of the last command executed	Table 51 on page 45
0Bh	CollPos	bit position of the first bit-collision detected on the RF interface	Table 53 on page 46
0Ch	TimerValue	value of the timer	Table 55 on page 46
0Dh	CRCResultLSB	LSB of the CRC coprocessor register	Table 57 on page 47
0Eh	CRCResultMSB	MSB of the CRC coprocessor register	Table 59 on page 47
0Fh	PreSet0F	these values must not be changed	Table 61 on page 47
Page 2: Transmitter and coder control			
10h	Page	selects the page register	Table 33 on page 40
11h	TxControl	controls the operation of the antenna driver pins TX1 and TX2	Table 63 on page 48
12h	CwConductance	selects the conductance of the antenna driver pins TX1 and TX2	Table 65 on page 49
13h	ModConductance	defines the conductance of the output driver pins TX1 and TX2 during modulation	Table 67 on page 49
14h	CoderControl	sets the bit encoding mode and framing during transmission	Table 69 on page 50
15h	ModWidth	selects the modulation pulse width	Table 71 on page 51
16h	ModWidthSOF	selects the SOF pulse-width modulation (ICODE1 fast mode)	Table 73 on page 51
17h	PreSet17	these values must not be changed	Table 75 on page 51
Page 3: Receiver and decoder control			
18	Page	selects the page register	Table 33 on page 40
19	RxControl1	controls receiver behavior	Table 76 on page 52
1A	DecoderControl	controls decoder behavior	Table 78 on page 52
1B	BitPhase	selects the bit-phase between transmitter and receiver clock	Table 80 on page 53
1C	RxThreshold	selects thresholds for the bit decoder	Table 82 on page 53
1D	PreSet1D	these values must not be changed	Table 84 on page 54
1Eh	RxControl2	controls decoder and defines the receiver input source	Table 85 on page 54
1Fh	ClockQControl	clock control for the 90° phase-shifted Q-channel clock	Table 87 on page 54

Table 31. FSV9504 register overview

Sub address (Hex)	Register name	Function	Refer to
Page 4: RF Timing and channel redundancy			
20h	Page	selects the page register	Table 33 on page 40
21h	RxWait	selects the interval after transmission before the receiver starts	Table 89 on page 55
22h	ChannelRedundancy	selects the method and mode used to check data integrity on the RF channel	Table 91 on page 55
23h	CRCPresetLSB	preset LSB value for the CRC register	Table 93 on page 56
24h	CRCPresetMSB	preset MSB value for the CRC register	Table 95 on page 56
25h	TimeSlotPeriod	selects the time between automatically transmitted frames	Table 97 on page 57
26h	SIGOUTSelect	selects internal signal applied to pin SIGOUT, includes the MSB of value TimeSlotPeriod; see Table 97 on page 57	Table 99 on page 57
27h	PreSet27	these values are not changed	Table 101 on page 58
Page 5: FIFO, timer and IRQ pin configuration			
28h	Page	selects the page register	Table 33 on page 40
29h	FIFOLevel	defines the FIFO buffer overflow and underflow warning levels	Table 41 on page 42
2Ah	TimerClock	selects the timer clock divider	Table 104 on page 59
2Bh	TimerControl	selects the timer start and stop conditions	Table 106 on page 59
2Ch	TimerReload	defines the timer preset value	Table 108 on page 60
2Dh	IRQPinConfig	configures pin IRQ output stage	Table 110 on page 60
2Eh	PreSet2E	these values are not changed	Table 112 on page 60
2Fh	PreSet2F	these values are not changed	Table 113 on page 60
Page 6: reserved registers			
30h	Page	selects the page register	Table 33 on page 40
31h	reserved	reserved	Table 114 on page 61
32h	reserved	reserved	
33h	reserved	reserved	
34h	reserved	reserved	
35h	reserved	reserved	
36h	reserved	reserved	
37h	reserved	reserved	
Page 7: Test control			
38h	Page	selects the page register	Table 33 on page 40
39h	reserved	reserved	Table 115 on page 61
3Ah	TestAnaSelect	selects analog test mode	Table 116 on page 61
3Bh	PreSet3B	reserved	Table 118 on page 62
3Ch	PreSet3C	reserved	Table 119 on page 62
3Dh	TestDigiSelect	selects digital test mode	Table 120 on page 62
3Eh	reserved	reserved	Table 122 on page 63
3Fh	reserved	reserved	

9.4 FSV9504 register flags overview

Table 32. FSV9504 register flags overview

Flag(s)	Register	Bit	Address
AccessErr	ErrorFlag	5	0Ah
BitPhase[7:0]	BitPhase	7 to 0	1Bh
ClkQ180Deg	ClockQControl	7	1Fh
ClkQCalib	ClockQControl	6	1Fh
ClkQDelay[4:0]	ClockQControl	4 to 0	1Fh
CollErr	ErrorFlag	0	0Ah
CollLevel[3:0]	RxThreshold	3 to 0	1Ch
CollPos[7:0]	CollPos	7 to 0	0Bh
Command[5:0]	Command	5 to 0	01h
CRC3309	ChannelRedundancy	5	22h
CRC8	ChannelRedundancy	4	22h
CRCErr	ErrorFlag	3	0Ah
CRCMSBFirst	ChannelRedundancy	6	22h
CRCPresetLSB[7:0]	CRCPresetLSB	7 to 0	23h
CRCPresetMSB[7:0]	CRCPresetMSB	7 to 0	24h
CRCReady	SecondaryStatus	5	05h
CRCResultMSB[7:0]	CRCResultMSB	7 to 0	0Eh
CRCResultLSB[7:0]	CRCResultLSB	7 to 0	0Dh
DecoderSource[1:0]	RxControl2	1 to 0	1Eh
E2Ready	SecondaryStatus	6	05h
Err	PrimaryStatus	2	03h
FIFOData[7:0]	FIFOData	7 to 0	02h
FIFOLength[6:0]	FIFOLength	7 to 0	04h
FIFOOvfl	ErrorFlag	4	0Ah
FlushFIFO	Control	0	09h
FramingErr	ErrorFlag	2	0Ah
Gain[1:0]	RxControl1	1 to 0	19h
GsCfgCW[5:0]	CwConductance	5 to 0	12h
GsCfgMod[5:0]	ModConductance	5 to 0	13h
HiAlert	PrimaryStatus	1	03h
HiAlertIEn	InterruptEn	1	06h
HiAlertIRq	InterruptRq	1	07h
IdleIEn	InterruptEn	2	06h
IdleIRq	InterruptRq	2	07h
IFDetectBusy	Command	7	01h
IRq	PrimaryStatus	3	03h
IRQInv	IRQPinConfig	1	2Dh
IRQPushPull	IRQPinConfig	0	2Dh
LoAlert	PrimaryStatus	0	03h

Table 32. FSV9504 register flags overview

Flag(s)	Register	Bit	Address
LoAlertIEn	InterruptEn	0	06h
LoAlertIRq	InterruptRq	0	07h
SIGOUTSelect[2:0]	SIGOUTSelect	2 to 0	26h
MinLevel[3:0]	RxThreshold	7 to 4	1Ch
ModemState[2:0]	PrimaryStatus	6 to 4	03h
ModulatorSource[1:0]	TxControl	6 to 5	11h
ModWidth[7:0]	ModWidth	7 to 0	15h
PageSelect[2:0]	Page	2 to 0	00h, 08h, 10h, 18h, 20h, 28h, 30h and 38h
PowerDown	Control	4	09h
RcvClkSell	RxControl2	7	1Eh
RxAutoPD	RxControl2	6	1Eh
RxCRCEn	ChannelRedundancy	3	22h
RxIEn	InterruptEn	3	06h
RxIRq	InterruptRq	3	07h
RxLastBits[2:0]	SecondaryStatus	2 to 0	05h
RxWait[7:0]	RxWait	7 to 0	21h
SetIEn	InterruptEn	7	06h
SetIRq	InterruptRq	7	07h
SignalToSIGOUT	TestDigiSelect	7	3Dh
StandBy	Control	5	09h
TAutoRestart	TimerClock	5	2Ah
TestAnaOutSel[4:0]	TestAnaSelect	3 to 0	3Ah
TestDigiSignalSel[6:0]	TestDigiSelect	6 to 0	3Dh
TimerIEn	InterruptEn	5	06h
TimerIRq	InterruptRq	5	07h
TimerValue[7:0]	TimerValue	7 to 0	0Ch
TPreScaler[4:0]	TimerClock	4 to 0	2Ah
TReloadValue[7:0]	TimerReload	7 to 0	2Ch
TRunning	SecondaryStatus	7	05h
TStartTxBegin	TimerControl	0	2Bh
TStartTxEnd	TimerControl	1	2Bh
TStartNow	Control	1	09h
TStopRxBegin	TimerControl	2	2Bh
TStopRxEnd	TimerControl	3	2Bh
TStopNow	Control	2	09h
TX1RFEn	TxControl	0	11h
TX2Cw	TxControl	2	11h
TX2Inv	TxControl	3	11h
TX2RFEn	TxControl	1	11h
TxCRCEn	ChannelRedundancy	2	22h

Table 32. FSV9504 register flags overview

Flag(s)	Register	Bit	Address
TxIEn	InterruptEn	4	06h
TxIRq	InterruptRq	4	07h
TxLastBits[2:0]	BitFraming	2 to 0	0Fh
UsePageSelect	Page	7	00h, 08h, 10h, 18h, 20h, 28h, 30h and 38h
WaterLevel[5:0]	FIFOLevel	5 to 0	29h
ZeroAfterColl	DecoderControl	5	1Ah

9.5 Register descriptions

9.5.1 Page 0: Command and status

9.5.1.1 Page register

Selects the page register.

Table 33. Page register (address: 00h, 08h, 10h, 18h, 20h, 28h, 30h, 38h) reset value: 1000 0000b, 80h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	UsePageSelect	0000				PageSelect[2:0]		
Access	R/W	R/W				R/W	R/W	R/W

Table 34. Page register bit descriptions

Bit	Symbol	Value	Description
7	UsePageSelect	1	the value of PageSelect[2:0] is used as the register address A5, A4, and A3. The LSBs of the register address are defined using the address pins or the internal address latch, respectively.
		0	the complete content of the internal address latch defines the register address. The address pins are used as described in Table 4 on page 7.
6 to 3	0000	-	reserved
2 to 0	PageSelect[2:0]	-	when UsePageSelect = logic 1, the value of PageSelect is used to specify the register page (A5, A4 and A3 of the register address)

9.5.1.2 Command register

Starts and stops the command execution.

Table 35. Command register (address: 01h) reset value: x000 0000b, x0h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	IFDetectBusy	0	Command[5:0]					
Access	R	R	D					

Table 36. Command register bit descriptions

Bit	Symbol	Value	Description
7	IFDetectBusy	-	shows the status of interface detection logic
		0	interface detection finished successfully
		1	interface detection ongoing
6	0	-	reserved
5 to 0	Command[5:0]	-	activates a command based on the Command code. Reading this register shows which command is being executed.

9.5.1.3 FIFOData register

Input and output of the 64 byte FIFO buffer.

Table 37. FIFOData register (address: 02h) reset value: xxxx xxxxb, xxh bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	FIFOData[7:0]							
Access	D							

Table 38. FIFOData register bit descriptions

Bit	Symbol	Description
7 to 0	FIFOData[7:0]	data input and output port for the internal 64-byte FIFO buffer. The FIFO buffer acts as a parallel in to parallel out converter for all data streams.

9.5.1.4 PrimaryStatus register

Bits relating to receiver, transmitter and FIFO buffer status flags.

Table 39. PrimaryStatus register (address: 03h) reset value: 0000 0001b, 01h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	0	ModemState[2:0]			IRq	Err	HiAlert	LoAlert
Access	R	R			R	R	R	R

Table 40. PrimaryStatus register bit descriptions

Bit	Symbol	Value	Status	Description
7	0	-		reserved
6 to 4	ModemState[2:0]			shows the state of the transmitter and receiver state machines:
		000	Idle	neither the transmitter or receiver are operating; neither of them are started or have input data
		001	TxSOF	transmit start of frame pattern
		010	TxData	transmit data from the FIFO buffer (or redundancy CRC check bits)
		011	TxEOF	transmit End Of Frame (EOF) pattern
		100	GoToRx1	intermediate state 1; receiver starts
			GoToRx2	intermediate state 2; receiver finishes
		101	PrepareRx	waiting until the RxWait register time period expires
		110	AwaitingRx	receiver activated; waiting for an input signal on pin RX
		111	Receiving	receiving data
3	IRq	-		shows any interrupt source requesting attention based on the InterruptEn register flag settings
2	Err	1		any error flag in the ErrorFlag register is set
1	HiAlert	1		the alert level for the number of bytes in the FIFO buffer (FIFOLength[6:0]) is: $HiAlert = 64 - FIFOLength \leq WaterLevel$ otherwise value = logic 0 Example: FIFOLength = 60, WaterLevel = 4 then HiAlert = logic 1 FIFOLength = 59, WaterLevel = 4 then HiAlert = logic 0
0	LoAlert	1		the alert level for number of bytes in the FIFO buffer (FIFOLength[6:0]) is: $LoAlert = FIFOLength \leq WaterLevel$ otherwise value = logic 0 Example: FIFOLength = 4, WaterLevel = 4 then LoAlert = logic 1 FIFOLength = 5, WaterLevel = 4 then LoAlert = logic 0

9.5.1.5 FIFOLength register

Number of bytes in the FIFO buffer.

Table 41. FIFOLength register (address: 04h) reset value: 0000 0000b, 00h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	0	FIFOLength[6:0]						
Access	R	R						

Table 42. FIFOLength bit descriptions

Bit	Symbol	Description
7	0	reserved
6 to 0	FIFOLength[6:0]	gives the number of bytes stored in the FIFO buffer. Writing increments the FIFOLength register value while reading decrements the FIFOLength register value

9.5.1.6 SecondaryStatus register

Various secondary status flags.

Table 43. SecondaryStatus register (address: 05h) reset value: 01100 000b, 60h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	TRunning	E2Ready	CRCReady	00		RxLastBits[2:0]		
Access	R	R	R	R		R		

Table 44. SecondaryStatus register bit descriptions

Bit	Symbol	Value	Description
7	TRunning	1	the timer unit is running and the counter decrements the TimerValue register on the next timer clock cycle
		0	the timer unit is not running
6	E2Ready	1	EEPROM programming is finished
		0	EEPROM programming is ongoing
5	CRCReady	1	CRC calculation is finished
		0	CRC calculation is ongoing
4 to 3	00	-	reserved
2 to 0	RxLastBits [2:0]	-	shows the number of valid bits in the last received byte. If zero, the whole byte is valid

9.5.1.7 InterruptEn register

Control bits to enable and disable passing of interrupt requests.

Table 45. InterruptEn register (address: 06h) reset value: 0000 0000b, 00h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	SetIEn	0	TimerIEn	TxIEn	RxIEn	IdleIEn	HiAlertIEn	LoAlertIEn
Access	W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 46. InterruptEn register bit descriptions

Bit	Symbol	Value	Description
7	SetIEn	1	indicates that the marked bits in the InterruptEn register are set
		0	clears the marked bits
6	0	-	reserved
5	TimerIEn	-	sends the TimerIRq timer interrupt request to pin IRQ[1]
4	TxIEn	-	sends the TxIRq transmitter interrupt request to pin IRQ[1]
3	RxIEn	-	sends the RxIRq receiver interrupt request to pin IRQ[1]

Table 46. InterruptEn register bit descriptions

Bit	Symbol	Value	Description
2	IdleIEn	-	sends the IdleIRq idle interrupt request to pin IRQ[1]
1	HiAlertIEn	-	sends the HiAlertIRq high alert interrupt request to pin IRQ[1]
0	LoAlertIEn	-	sends the LoAlertIRq low alert interrupt request to pin IRQ[1]

[1] This bit can only be set or cleared using bit SetIEn.

9.5.1.8 InterruptRq register

Interrupt request flags.

Table 47. InterruptRq register (address: 07h) reset value: 0000 0000b, 00h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	SetIRq	0	TimerIRq	TxIRq	RxIRq	IdleIRq	HiAlertIRq	LoAlertIRq
Access	W	R/W	D	D	D	D	D	D

Table 48. InterruptRq register bit descriptions

Bit	Symbol	Value	Description
7	SetIRq	1	sets the marked bits in the InterruptRq register
		0	clears the marked bits in the InterruptRq register
6	0	-	reserved
5	TimerIRq	1	timer decrements the TimerValue register to zero
		0	timer decrements are still greater than zero
4	TxIRq	1	TxIRq is set to logic 1 if one of the following events occurs: Transceive command; all data transmitted CalcCRC command; all data is processed WriteE2 command; all data is programmed
		0	when not acted on by Transceive, CalcCRC or WriteE2 commands
3	RxIRq	1	the receiver terminates
		0	reception still ongoing
2	IdleIRq	1	command terminates correctly. For example; when the Command register changes its value from any command to the Idle command. If an unknown command is started the IdleIRq bit is set. Microprocessor start-up of the Idle command does not set the IdleIRq bit.
		0	IdleIRq = logic 0 in all other instances
1	HiAlertIRq	1	PrimaryStatus register HiAlert bit is set[1]
		0	PrimaryStatus register HiAlert bit is not set
0	LoAlertIRq	1	PrimaryStatus register LoAlert bit is set[1]
		0	PrimaryStatus register LoAlert bit is not set

[1] PrimaryStatus register Bit HiAlertIRq stores this event and it can only be reset using bit SetIRq.

9.5.2 Page 1: Control and status

9.5.2.1 Page register

Selects the page register; see Section 9.5.1.1 “Page register” on page 40.

9.5.2.2 Control register

Various control flags, for timer, power saving, etc.

Table 49. Control register (address: 09h) reset value: 0000 0000b, 00h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	00		StandBy	PowerDown	0	TStopNow	TStartNow	FlushFIFO
Access	R/W		D	D	D	W	W	W

Table 50. Control register bit descriptions

Bit	Symbol	Value	Description
7 to 6	00	-	reserved
5	StandBy	1	activates Standby mode. The current consuming blocks are switched off but the clock keeps running
4	PowerDown	1	activates Soft Power-down mode. The current consuming blocks are switched off including the clock
3	0	-	reserved
2	TStopNow	1	immediately stops the timer. Reading this bit always returns logic 0
1	TStartNow	1	immediately starts the timer. Reading this bit will always returns logic 0
0	FlushFIFO	1	immediately clears the internal FIFO buffer’s read and write pointer, the FIFOLength[6:0] bits are set to logic 0 and the FIFOOvfl flag. Reading this bit always returns logic 0

9.5.2.3 ErrorFlag register

Error flags show the error status of the last executed command.

Table 51. ErrorFlag register (address: 0Ah) reset value: 0100 0000b, 00h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	0	0	AccessErr	FIFOOvfl	CRCErr	FramingErr	0	CollErr
Access	R	R	R	R	R	R	R	R

Table 52. ErrorFlag register bit descriptions

Bit	Symbol	Value	Description
7 to 6	0	-	reserved
5	AccessErr	1	set when the access rights to the EEPROM are violated
		0	set when an EEPROM related command starts
4	FIFOOvfl	1	set when the microprocessor or FSV9504 internal state machine (e.g. receiver) tries to write data to the FIFO buffer when it is full
3	CRCErr	1	set when RxCRCEn is set and the CRC fails
		0	automatically set during the PrepareRx state in the receiver start phase

Table 52. ErrorFlag register bit descriptions

Bit	Symbol	Value	Description
2	FramingErr	1	set when the SOF is incorrect
		0	automatically set during the PrepareRx state in the receiver start phase
1	0	-	reserved
0	CollErr	1	set when a bit-collision is detected
		0	automatically set during the PrepareRx state in the receiver start phase

9.5.2.4 CollPos register

Bit position of the first bit-collision detected on the RF interface.

Table 53. CollPos register (address: 0Bh) reset value: 0000 0000b, 00h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	CollPos[7:0]							
Access	R							

Table 54. CollPos register bit descriptions

Bit	Symbol	Description
7 to 0	CollPos[7:0]	this register shows the bit position of the first detected collision in a received frame. Example: 00h indicates a bit collision in the start bit 01h indicates a bit collision in the 1st bit ... 08h indicates a bit collision in the 8th bit

9.5.2.5 TimerValue register

Value of the timer.

Table 55. TimerValue register (address: 0Ch) reset value: xxxx xxxxb, xxh bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	TimerValue[7:0]							
Access	R							

Table 56. TimerValue register bit descriptions

Bit	Symbol	Description
7 to 0	TimerValue[7:0]	this register shows the timer counter value

9.5.2.6 CRCResultLSB register

LSB of the CRC coprocessor register.

Table 57. CRCResultLSB register (address: 0Dh) reset value: xxxx xxxxb, xxh bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	CRCResultLSB[7:0]							
Access	R							

Table 58. CRCResultLSB register bit descriptions

Bit	Symbol	Description
7 to 0	CRCResultLSB[7:0]	gives the CRC register's least significant byte value; only valid if CRCReady = logic 1

9.5.2.7 CRCResultMSB register

MSB of the CRC coprocessor register.

Table 59. CRCResultMSB register (address: 0Eh) reset value: xxxx xxxxb, xxh bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	CRCResultMSB[7:0]							
Access	R							

Table 60. CRCResultMSB register bit descriptions

Bit	Symbol	Description
7 to 0	CRCResultMSB[7:0]	gives the CRC register's most significant byte value; only valid if CRCReady = logic 1. The register's value is undefined for 8-bit CRC calculation.

9.5.2.8 BitFraming register

Adjustments for bit oriented frames.

Table 61. BitFraming register (address: 0Fh) reset value: 0000 0000b, 00h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	0	RxAlign[2:0]			0	TxLastBits[2:0]		
Access	R/W	D			R/W	D		

Table 62. BitFraming register bit descriptions

Bit	Symbol	Value	Description
7	0	-	reserved
6 to 4	RxAlign[2:0]		defines the bit position for the first bit received to be stored in the FIFO buffer. Additional received bits are stored in the next subsequent bit positions. After reception, RxAlign[2:0] is automatically cleared. For example:
		000	the LSB of the received bit is stored in bit position 0 and the second received bit is stored in bit position 1
		001	the LSB of the received bit is stored in bit position 1, the second received bit is stored in bit position 2
		...	
		111	the LSB of the received bit is stored in bit position 7, the second received bit is stored in the next byte in bit position 0
3	0	-	reserved
2 to 0	TxLastBits[2:0]	-	defines the number of bits of the last byte that shall be transmitted. 000 indicates that all bits of the last byte will be transmitted. TxLastBits[2:0] is automatically cleared after transmission.

9.5.3 Page 2: Transmitter and control

9.5.3.1 Page register

Selects the page register; see Section 9.5.1.1 “Page register” on page 40.

9.5.3.2 TxControl register

Controls the logical behavior of the antenna pin TX1 and TX2.

Table 63. TxControl register (address: 11h) reset value: 0100 1000b, 48h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	0	ModulatorSource [1:0]		Force 100ASK	TX2Inv	TX2Cw	TX2RFEn	TX1RFEn
Access	R/W	R/W		R/W	R/W	R/W	R/W	R/W

Table 64. TxControl register bit descriptions

Bit	Symbol	Value	Description
7	0	-	this value must not be changed
6 to 5	ModulatorSource[1:0]		selects the source for the modulator input:
		00	modulator input is LOW
		01	modulator input is HIGH
		10	modulator input is the internal encoder
		11	reserved
4	Force100ASK	1	forces a 100 % ASK modulation independent of the ModConductance register setting
3	TX2Inv	1	the output signal on pin TX2 is an inverted 13.56 MHz carrier

Table 64. TxControl register bit descriptions

Bit	Symbol	Value	Description
2	TX2Cw	1	the output on pin TX2 is a continuously unmodulated 13.56 MHz carrier
		0	enables modulation of the 13.56 MHz carrier signal
1	TX2RFEn	1	the output signal on pin TX2 is the 13.56 MHz carrier modulated by the transmission data
		0	TX2 is driven at a constant output level
0	TX1RFEn	1	the output signal on pin TX1 is the 13.56 MHz carrier modulated by the transmission data
		0	TX1 is driven at a constant output level

9.5.3.3 CwConductance register

Selects the conductance of the antenna driver pins TX1 and TX2.

Table 65. CwConductance register (address: 12h) reset value: 0011 1111b, 3Fh bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	00		GsCfgCW[5:0]					
Access	R/W	R/W	R/W					

Table 66. CwConductance register bit descriptions

Bit	Symbol	Description
7 to 6	00	these values must not be changed
5 to 0	GsCfgCW[5:0]	defines the Cwconductance register value for the output driver. This can be used to regulate the output power/current consumption and operating distance.

See Section 8.9.3 on page 25 for detailed information about GsCfgCW[5:0].

9.5.3.4 ModConductance register

Defines the driver output conductance.

Table 67. ModConductance register (address: 13h) reset value: 0000 0101b, 05h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	00		GsCfgMod[5:0]					
Access	R/W	R/W	R/W					

Table 68. ModConductance register bit descriptions

Bit	Symbol	Description
7 to 6	00	these values must not be changed
5 to 0	GsCfgMod[5:0]	defines the ModConductance register value for the output driver during modulation. This is used to regulate the modulation index.

See Section 8.9.3 on page 25 for detailed information about GsCfgMod[5:0].

9.5.3.5 CoderControl register

Sets the clock rate and the coding mode.

Table 69. CoderControl register (address: 14h) reset value: 0010 1100b, 2Ch bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	SendOnePulse	0	CoderRate[2:0]			TxCoding[2:0]		
Access	R/W	R/W	R/W			R/W		

Table 70. CoderControl register bit descriptions

Bit	Symbol	Value	Description
7	SendOnePulse	1	forces ISO/IEC 15693 modulation. Used to switch to the next TimeSlotPeriod if the Inventory command is used. This bit is not cleared automatically, it must be reset by the user to logic 0.
6	0	-	this value must not be changed
5 to 3	CoderRate[2:0]		this register defines the clock rate for the encoder circuit
		000	reserved
		001	reserved
		010	reserved
		011	reserved
		100	~106 kHz
		101	ICODE1 standard mode and ISO/IEC 15693 (~52.97 kHz)
		110	ICODE1 fast mode (~26.48 kHz)
		111	reserved
2 to 0	TxCoding[2:0]		this register defines the bit coding mode and framing during transmission
		000	reserved
		001	reserved
		010	reserved
		011	reserved
		100	ICODE1 standard mode (1 out of 256 coding)
		101	ICODE1 fast mode (RZ coding)
		110	ISO/IEC 15693 standard mode (1 out of 256 coding)
		111	ISO/IEC 15693 fast mode (1 out of 4 coding)

9.5.3.6 ModWidth register

Selects the pulse-modulation width.

Table 71. ModWidth register (address: 15h) reset value: 0011 1111b, 3Fh bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	ModWidth[7:0]							
Access	R/W							

Table 72. ModWidth register bit descriptions

Bit	Symbol	Description
7 to 0	ModWidth[7:0]	defines the width of the modulation pulse based on t_{mod} = 2 × (ModWidth + 1) / f_{clk} where f_{clk} = 13.56 MHz oscillator clock. Preset for ICODE1 (fast and standard modes) and ISO/IEC 15693 is 3Fh: modulation width = 9.44 µs.

9.5.3.7 ModWidthSOF register

Table 73. ModWidthSOF register (address: 16h) reset value: 0011 1111b, 3Fh bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	ModWidthSOF[7:0]							
Access	R/W							

Table 74. ModWidthSOF register bit descriptions

Bit	Symbol	Value	Description
7 to 0	ModWidthSOF		defines the width of the modulation pulse for SOF as t_{mod} = 2 × (ModWidth + 1) / f_{clk} the register settings are:
		3Fh	ICODE1 standard mode; modulation width SOF = 9.44 µs
		73h	ICODE1 fast mode; modulation width SOF = 18.88 µs
		3Fh	ISO/IEC 15693; modulation width SOF = 9.44 µs

9.5.3.8 PreSet17 register

These bit values must not be changed.

Table 75. PreSet17 register (address: 17h) reset value: 0000 0000b, 00h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	0	0	0	0	0	0	0	0
Access	R/W							

9.5.4 Page 3: Receiver and decoder control

9.5.4.1 Page register

Selects the page register; see Section 9.5.1.1 “Page register” on page 40.

9.5.4.2 RxControl1 register

Controls receiver operation.

Table 76. RxControl1 register (address: 19h) reset value: 1000 1011b, 8Bh bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	SubCPulses[2:0]			0	1	0	Gain[1:0]	
Access	R/W			R/W	R/W	R/W	R/W	

Table 77. RxControl1 register bit descriptions

Bit	Symbol	Value	Description
7 to 5	SubCPulses[2:0]		defines the number of subcarrier pulses for each bit
		000	reserved
		001	reserved
		010	reserved
		011	8 pulses for each bit ICODE SLI (fast inventory read, 53 kBd)
		100	16 pulses for each bit ICODE1, ISO/IEC 15693
		101	reserved
		110	reserved
		111	reserved
4 to 2	010		these values must not be changed
2	LPOff		switches off a low-pass filter at the internal amplifier
1 to 0	Gain[1:0]		defines the receiver's signal voltage gain factor
		00	27 dB gain factor
		01	31 dB gain factor
		10	38 dB gain factor
		11	42 dB gain factor

9.5.4.3 DecoderControl register

Controls decoder operation.

Table 78. DecoderControl register (address: 1Ah) reset value: 0000 0000b, 00h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	0	RxMultiple	ZeroAfterColl	RxFraming[1:0]		RxInvert	0	0
Access	R/W	R/W	R/W	R/W		R/W	R/W	R/W

Table 79. DecoderControl register bit descriptions

Bit	Symbol	Value	Description
7	0	-	this value must not be changed
6	RxMultiple	0	after receiving one frame, the receiver is deactivated
		1	enables reception of more than one frame
5	ZeroAfterColl	1	any bits received after a bit-collision are masked to zero. This helps to resolve the anti-collision procedure as defined in ISO/IEC 15693

Table 79. DecoderControl register bit descriptions

Bit	Symbol	Value	Description
4 to 3	RxFraming[1:0]		selects the received frame type
		00	ICODE1
		01	reserved
		10	ISO/IEC 15693
		11	reserved
2	RxInvert	0	modulation at the first half-bit results in logic 1 (ICODE1)
		1	modulation at the first half-bit results in logic 0 (ISO/IEC 15693)
1 to 0	00	-	these values must not be changed

9.5.4.4 BitPhase register

Selects the bit-phase between transmitter and receiver clock.

Table 80. BitPhase register (address: 1Bh) reset value: 0101 0100b, 54h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	BitPhase[7:0]							
Access	R/W							

Table 81. BitPhase register bit descriptions

Bit	Symbol	Description
7 to 0	BitPhase	defines the phase relationship between transmitter and receiver clock **Remark:** The correct value of this register is essential for proper operation.

9.5.4.5 RxThreshold register

Selects thresholds for the bit decoder.

Table 82. RxThreshold register (address: 1Ch) reset value: 0110 1000b, 68h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	MinLevel[3:0]				CollLevel[3:0]			
Access	R/W				R/W			

Table 83. RxThreshold register bit descriptions

Bit	Symbol	Description
7 to 4	MinLevel[3:0]	the minimum signal strength the decoder will accept. If the signal strength is below this level, it is not evaluated.
3 to 0	CollLevel[3:0]	the minimum signal strength at the decoder input that must be reached by the weaker half-bit of the Manchester encoded signal to generate a bit-collision (relative to the amplitude of the stronger half-bit)

9.5.4.6 PreSet1D register

These values must not be changed.

Table 84. BPSKDemControl register (address: 1Dh) reset value: 0000 0000b, 00h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	0	0	0	0	0	0	0	0
Access	R/W							

9.5.4.7 RxControl2 register

Controls decoder operation and defines the input source for the receiver.

Table 85. RxControl2 register (address: 1Eh) reset value: 0100 0001b, 41h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	RcvClkSell	RxAutoPD	0000				DecoderSource[1:0]	
Access	R/W	R/W	R/W				R/W	

Table 86. RxControl2 register bit descriptions

Bit	Symbol	Value	Description
7	RcvClkSell	1	I-clock is used as the receiver clock[1]
		0	Q-clock is used as the receiver clock[1]
6	RxAutoPD	1	receiver circuit is automatically switched on before receiving and switched off afterwards. This can be used to reduce current consumption.
		0	receiver is always activated
5 to 2	0000	-	these values must not be changed
1 to 0	DecoderSource[1:0]		selects the source for the decoder input
		00	LOW
		01	internal demodulator
		10	reserved
		11	reserved

[1] I-clock and Q-clock are 90° phase-shifted from each other.

9.5.4.8 ClockQControl register

Controls clock generation for the 90° phase-shifted Q-clock.

Table 87. ClockQControl register (address: 1Fh) reset value: 000x xxxxb, xxh bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	ClkQ180Deg	ClkQCalib	0	ClkQDelay[4:0]				
Access	R	R/W	R/W	D				

Table 88. ClockQControl register bit descriptions

Bit	Symbol	Value	Description
7	ClkQ180Deg	1	Q-clock is phase-shifted more than 180° compared to the I-clock
		0	Q-clock is phase-shifted less than 180° compared to the I-clock

Table 88. ClockQControl register bit descriptions

Bit	Symbol	Value	Description
6	ClkQCalib	0	Q-clock is automatically calibrated after the reset phase and after data reception from the label
		1	no calibration is performed automatically
5	0	-	this value must not be changed
4 to 0	ClkQDelay[4:0]	-	this register shows the number of delay elements used to generate a 90° phase-shift of the I-clock to obtain the Q-clock. It can be written directly by the microprocessor or by the automatic calibration cycle.

9.5.5 Page 4: RF Timing and channel redundancy

9.5.5.1 Page register

Selects the page register; see Section 9.5.1.1 “Page register” on page 40.

9.5.5.2 RxWait register

Selects the time interval after transmission, before the receiver starts.

Table 89. RxWait register (address: 21h) reset value: 0000 1000b, 08h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	RxWait[7:0]							
Access	R/W							

Table 90. RxWait register bit descriptions

Bit	Symbol	Function
7 to 0	RxWait[7:0]	after data transmission, the activation of the receiver is delayed for RxWait bit-clock cycles. During this frame guard time any signal on pin RX is ignored.

9.5.5.3 ChannelRedundancy register

Selects the type and mode of checking the RF channel data integrity.

Table 91. ChannelRedundancy register (address: 22h) reset value: 0000 1100b, 0Ch bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	0	CRCMSB First	CRC3309	CRC8	RxCRCEn	TxCRCEn	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 92. ChannelRedundancy bit descriptions

Bit	Symbol	Value	Function
7	0	-	this value must not be changed
6	CRCMSBFirst	1	CRC calculation shifts the MSB into the CRC coprocessor first[1]
		0	CRC calculation starts with the LSB

Table 92. ChannelRedundancy bit descriptions

Bit	Symbol	Value	Function
5	CRC3309	1	CRC calculation is performed using ISO/IEC 3309 as defined by ISO/IEC 15693[1]
		0	CRC calculation is performed using ICODE1
4	CRC8	1	an 8-bit CRC is calculated
		0	a 16-bit CRC is calculated
3	RxCRCEn	1	the last byte(s) of a received frame are interpreted as CRC bytes. If the CRC is correct, the CRC bytes are not passed to the FIFO. If the CRC bytes are incorrect, the CRCErr flag is set.
		0	no CRC is expected
2	TxCRCEn	1	CRC is calculated over the transmitted data and the CRC bytes are appended to the data stream
		0	no CRC is transmitted
1 to 0	00	-	reserved

[1] When used with ISO/IEC 15693, this bit must be set to logic 0.

9.5.5.4 CRCPresetLSB register

LSB of the preset value for the CRC register.

Table 93. CRCPresetLSB register (address: 23h) reset value: 1111 1110b, FEh bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	CRCPresetLSB[7:0]							
Access	R/W							

Table 94. CRCPresetLSB register bit descriptions

Bit	Symbol	Description
7 to 0	CRCPresetLSB[7:0]	defines the start value for CRC calculation. This value is loaded into the CRC at the beginning of transmission, reception and the CalcCRC command (if CRC calculation is enabled). The preset value is set for ICODE1.[1]

[1] To use the ISO/IEC 15693 functionality, the CRCPresetLSB register has to be set to FFh.

9.5.5.5 CRCPresetMSB register

MSB of the preset value for the CRC register.

Table 95. CRCPresetMSB register (address: 24h) reset value: 1111 1111b, FFh bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	CRCPresetMSB[7:0]							
Access	R/W							

Table 96. CRCPresetMSB bit descriptions [1]

Bit	Symbol	Description
7 to 0	CRCPresetMSB[7:0]	defines the starting value for CRC calculation. This value is loaded into the CRC at the beginning of transmission, reception and the CalcCRC command (if the CRC calculation is enabled) **Remark:** The preset value is the same for both ICODE1 and ISO/IEC 15693.

[1] This register is not relevant if CRC8 is set to logic 1.

9.5.5.6 TimeSlotPeriod register

Defines the time-slot period for ICODE1 protocol.

Table 97. TimeSlotPeriod register (address: 25h) reset value: 0000 0000b, 00h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	TimeSlotPeriod[7:0]							
Access	R/W							

Table 98. TimeSlotPeriod register bit descriptions

Bit	Symbol	Description
7 to 0	TimeSlotPeriod[7:0]	defines the time between automatically transmitted frames. To send a Quit frame using the ICODE1 protocol it is necessary to relate to the beginning of the command frame. The TimeSlotPeriod starts at the end of the command transmission. See Section 8.5.1.5 on page 19 for additional information.

9.5.5.7 SIGOUTSelect register

Selects the internal signal applied to pin SIGOUT.

Table 99. SIGOUTSelect register (address: 26h) reset value: 0000 0000b, 00h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	000			TimeSlotPeriodMSB	0	SIGOUTSelect[2:0]		
Access	R/W			R/W	R/W	R/W		

Table 100. SIGOUTSelect register bit descriptions

Bit	Symbol	Value	Description
7 to 5	000	-	these values must not be changed
4	TimeSlotPeriodMSB	-	MSB of value TimeSlotPeriod; see Table 97 on page 57 for more detailed information
3	0	-	this value must not be changed

Table 100. SIGOUTSelect register bit descriptions

Bit	Symbol	Value	Description
2 to 0	SIGOUTSelect[2:0]		defines which signal is routed to pin SIGOUT:
		000	constant LOW
		001	constant HIGH
		010	modulation signal (envelope) from the internal encoder
		011	serial data stream
		100	output signal of the carrier demodulator (label modulation signal)
		101	output signal of the subcarrier demodulator (Manchester encoded label signal)
		110	reserved
		111	reserved

9.5.5.8 PreSet27 register

These bit values must not be changed.

Table 101. PreSet27 (address: 27h) reset value: xxxx xxxxb, xxh bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

9.5.6 Page 5: FIFO, timer and IRQ pin configuration

9.5.6.1 Page register

Selects the page register; see Section 9.5.1.1 “Page register” on page 40.

9.5.6.2 FIFOLevel register

Defines the levels for FIFO underflow and overflow warning.

Table 102. FIFOLevel register (address: 29h) reset value: 0011 1110b, 3Eh bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	00		WaterLevel[5:0]					
Access	R/W		R/W					

Table 103. FIFOLevel register bit descriptions

Bit	Symbol	Description
7 to 6	00	these values must not be changed
5 to 0	WaterLevel[5:0]	defines, the warning level of a FIFO buffer overflow or underflow: HiAlert is set to logic 1 if the remaining FIFO buffer space is equal to, or less than, WaterLevel[5:0] bits in the FIFO buffer. LoAlert is set to logic 1 if equal to, or less than, WaterLevel[5:0] bits in the FIFO buffer.

9.5.6.3 TimerClock register

Selects the divider for the timer clock.

Table 104. TimerClock register (address: 2Ah) reset value: 0000 1011b, 0Bh bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	00		TAutoRestart	TPreScaler[4:0]				
Access	R/W		RW	RW				

Table 105. TimerClock register bit descriptions

Bit	Symbol	Value	Function
7 to 6	00	-	these values must not be changed
5	TAutoRestart	1	the timer automatically restarts its countdown from the TReloadValue[7:0] instead of counting down to zero
		0	the timer decrements to zero and register InterruptRq TimerIRq bit is set to logic 1
4 to 0	TPreScaler[4:0]	-	defines the timer clock frequency ($f_{TimerClock}$). The TPreScaler[4:0] can be adjusted from 0 to 15. The following formula is used to calculate the TimerClock frequency ($f_{TimerClock}$): $f_{TimerClock} = 13.56\ MHz / 2^{TPreScaler}$ [MHz]

9.5.6.4 TimerControl register

Selects start and stop conditions for the timer.

Table 106. TimerControl register (address: 2Bh) reset value: 0000 0010b, 02h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	0	0	0	0	TStopRxEnd	TStopRxBegin	TStartTxEnd	TStartTxBegin
Access	R/W				R/W	R/W	R/W	R/W

Table 107. TimerControl register bit descriptions

Bit	Symbol	Value	Description
7 to 4	0000	-	these values must not be changed
3	TStopRxEnd	1	the timer automatically stops when data reception ends
		0	the timer is not influenced by this condition
2	TStopRxBegin	1	the timer automatically stops when the first valid bit is received
		0	the timer is not influenced by this condition
1	TStartTxEnd	1	the timer automatically starts when data transmission ends. If the timer is already running, the timer restarts by loading TReloadValue[7:0] into the timer.
		0	the timer is not influenced by this condition
0	TStartTxBegin	1	the timer automatically starts when the first bit is transmitted. If the timer is already running, the timer restarts by loading TReloadValue[7:0] into the timer.
		0	the timer is not influenced by this condition

9.5.6.5 TimerReload register

Defines the preset value for the timer.

Table 108. TimerReload register (address: 2Ch) reset value: 0000 0000b, 00h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	TReloadValue[7:0]							
Access	R/W							

Table 109. TimerReload register bit descriptions

Bit	Symbol	Description
7 to 0	TReloadValue[7:0]	on a start event, the timer loads the TReloadValue[7:0] value. Changing this register only affects the timer on the next start event. If TReloadValue[7:0] is set to logic 0 the timer cannot start.

9.5.6.6 IRQPinConfig register

Configures the output stage for pin IRQ.

Table 110. IRQPinConfig register (address: 2Dh) reset value: 0000 0010b, 02h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	0	0	0	0	0	0	IRQInv	IRQPushPull
Access	R/W						R/W	R/W

Table 111. IRQPinConfig register bit descriptions

Bit	Symbol	Value	Description
7 to 2	000000	-	these values must not be changed
1	IRQInv	1	inverts the signal on pin IRQ with respect to bit IRq
		0	the signal on pin IRQ is not inverted and is the same as bit IRq
0	IRQPushPull	1	pin IRQ functions as a standard CMOS output pad
		0	pin IRQ functions as an open-drain output pad

9.5.6.7 PreSet2E register

These register bits must not be changed.

Table 112. PreSet2E register (address: 2Eh) reset value: 0000 0000b, 00h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

9.5.6.8 PreSet2F register

These register bits must not be changed.

Table 113. PreSet2F register (address: 2Fh) reset value: 0000 0000b, 00h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

9.5.7 Page 6: reserved

9.5.7.1 Page register

Selects the page register; see Section 9.5.1.1 “Page register” on page 40.

9.5.7.2 Reserved registers 31h, 32h, 33h, 34h, 35h, 36h and 37h

These registers are reserved for future use.

Table 114. Reserved registers (address: 31h, 32h, 33h, 34h, 35h, 36h, 37h) reset value: 0000 0000b, 00h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

9.5.8 Page 7: Test control

9.5.8.1 Page register

Selects the page register; see Section 9.5.1.1 “Page register” on page 40.

9.5.8.2 Reserved register 39h

This register is reserved for future use.

Table 115. Reserved register (address: 39h) reset value: 0000 0000b, 00h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	0	0	0	0	0	0	0	0
Access	W	W	W	W	W	W	W	W

9.5.8.3 TestAnaSelect register

Selects analog test signals.

Table 116. TestAnaSelect register (address: 3Ah) reset value: 0000 0000b, 00h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	0000				TestAnaOutSel[4:0]			
Access	W				W			

Table 117. TestAnaSelect bit descriptions

Bit	Symbol	Value	Description
7 to 4	0000	-	these values must not be changed
3 to 0	TestAnaOutSel[4:0]		selects the internal analog signal to be routed to pin AUX. See Section 14.2.2 on page 88 for detailed information. The settings are as follows:
		0	VMID
		1	Vbandgap
		2	VRxFollI
		3	VRxFollQ
		4	VRxAmpI
		5	VRxAmpQ
		6	VCorrNI
		7	VCorrNQ
		8	VCorrDI
		9	VCorrDQ
		A	VEvalL
		B	VEvalR
		C	VTemp
		D	reserved
		E	reserved
		F	reserved

9.5.8.4 PreSet3B register

These register bit values must not be changed.

Table 118. Reserved register (address: 3Bh) reset value: 0000 0000b, 00h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	0	0	0	0	0	0	0	0
Access	W	W	W	W	W	W	W	W

9.5.8.5 PreSet3C register

These register bit values must not be changed.

Table 119. Reserved register (address: 3Ch) reset value: 0000 0000b, 00h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	0	0	0	0	0	0	0	0
Access	W	W	W	W	W	W	W	W

9.5.8.6 TestDigiSelect register

Selects digital test mode.

Table 120. TestDigiSelect register (address: 3Dh) reset value: 0000 0000b, 00h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	SignalToSIGOUT	TestDigiSignalSel[6:0]						
Access	W	W						

Table 121. TestDigiSelect register bit descriptions

Bit	Symbol	Value	Description
7	SignalToSIGOUT	1	overrules the SIGOUTSelect[2:0] setting and routes the digital test signal defined with the TestDigiSignalSel[6:0] bits to pin SIGOUT
		0	SIGOUTSelect[2:0] defines the signal on pin SIGOUT
6 to 0	TestDigiSignalSel[6:0]	-	selects the digital test signal to be routed to pin SIGOUT. Refer to Section 14.2.3 on page 88 for detailed information. The following lists the signal names for the TestDigiSignalSel[6:0] addresses:
		74h	s_data
		64h	s_valid
		54h	s_coll
		44h	s_clock
		35h	rd_sync
		25h	wr_sync
		16h	int_clock

9.5.8.7 Reserved registers 3Eh, 3Fh

These registers are reserved for future use.

Table 122. Reserved register (address: 3Eh, 3Fh) reset value: 0000 0000b, 00h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

10. FSV9504 command set

FSV9504 operation is determined by an internal state machine capable of performing a command set. The commands can be started by writing the command code to the Command register. Arguments and/or data necessary to process a command are mainly exchanged using the FIFO buffer.

- Each command needing a data stream (or data byte stream) as an input immediately processes the data in the FIFO buffer
- Each command that requires arguments only starts processing when it has received the correct number of arguments from the FIFO buffer
- The FIFO buffer is not automatically cleared at the start of a command. It is, therefore, possible to write command arguments and/or the data bytes into the FIFO buffer before starting a command.
- Each command (except the StartUp command) can be interrupted by the microprocessor writing a new command code to the Command register e.g. the Idle command.

10.1 FSV9504 command overview

Table 123. FSV9504 commands overview

Command	Value	Action	FIFO communication	
			Arguments and data sent	Data received
StartUp	3Fh	runs the reset and initialization phase. See Section 10.1.2 on page 65. **Remark:** This command can only be activated by Power-On or Hard resets.	-	-
Idle	00h	no action; cancels execution of the current command. See Section 10.1.3 on page 66	-	-
Transmit	1Ah	transmits data from the FIFO buffer to the label. See Section 10.2.1 on page 66	data stream	-
Receive	16h	activates receiver circuitry. Before the receiver starts, the state machine waits until the time defined in the RxWait register has elapsed. See Section 10.2.2 on page 68. **Remark:** This command may be used for test purposes only, since there is no timing relationship to the Transmit command.	-	data stream
Transceive[1]	1Eh	transmits data from FIFO buffer to the label and automatically activates the receiver after transmission. The receiver waits until the time defined in the RxWait register has elapsed before starting. See Section 10.2.3 on page 70.	data stream	data stream
WriteE2	01h	reads data from the FIFO buffer and writes it to the EEPROM. See Section 10.3.1 on page 73.	start address LSB start address MSB data byte stream	-

Table 123. FSV9504 commands overview

Command	Value	Action	FIFO communication	
			Arguments and data sent	Data received
ReadE2	03h	reads data from the EEPROM and sends it to the FIFO buffer. See Section 10.3.2 on page 75. **Remark:** Keys cannot be read back	start address LSB start address MSB number of data bytes	data bytes
LoadConfig	07h	reads data from EEPROM and initializes the FSV9504 registers. See Section 10.4.1 on page 75.	start address LSB start address MSB	-
CalcCRC	12h	activates the CRC coprocessor **Remark:** The result of the CRC calculation is read from the CRCResultLSB and CRCResultMSB registers. See Section 10.4.2 on page 76.	data byte stream	-

[1] This command is the combination of the Transmit and Receive commands.

10.1.1 Basic states

10.1.2 StartUp command 3Fh

Table 124. StartUp command 3Fh

Command	Value	Action	Arguments and data	Returned data
StartUp	3Fh	runs the reset and initialization phase	-	-

Remark: This command can only be activated by a Power-On or Hard reset.

The StartUp command runs the reset and initialization phases. It does not need or return, any data. It cannot be activated by the microprocessor but is automatically started after one of the following events:

- Power-On Reset (POR) caused by power-up on pin DVDD
- POR caused by power-up on pin AVDD
- Negative edge on pin RSTPD

The reset phase comprises an asynchronous reset and configuration of certain register bits. The initialization phase configures several registers with values stored in the EEPROM.

When the StartUp command finishes, the Idle command is automatically executed.

Remark:

- The microprocessor must not write to the FSV9504 while it is still executing the StartUp command. To avoid this, the microprocessor polls for the Idle command to determine when the initialization phase has finished; see Section 8.7.4 on page 23.
- When the StartUp command is active, it is only possible to read from the Page 0 register.
- The StartUp command cannot be interrupted by the microprocessor.

10.1.3 Idle command 00h

Table 125. Idle command 00h

Command	Value	Action	Arguments and data	Returned data
Idle	00h	no action; cancels current command execution	-	-

The Idle command switches the FSV9504 to its inactive state where it waits for the next command. It does not need or return, any data.

The device automatically enters the idle state when a command finishes. When this happens, the FSV9504 sends an interrupt request by setting bit IdleIRq. When triggered by the microprocessor, the Idle command can be used to stop execution of all other commands (except the StartUp command) but this does not generate an interrupt request (IdleIRq).

Remark: Stopping command execution with the Idle command does not clear the FIFO buffer.

10.2 Commands for label communication

The FSV9504 is a fully ISO/IEC 15693 and ICODE1 compliant reader IC. Section 10.2.1 to Section 10.2.5 describe the command set for label communication and related communication protocols.

10.2.1 Transmit command 1Ah

Table 126. Transmit command 1Ah

Command	Value	Action	Arguments and data	Returned data
Transmit	1Ah	transmits data from FIFO buffer to label	data stream	-

The Transmit command reads data from the FIFO buffer and sends it to the transmitter. It does not return any data. The Transmit command can only be started by the microprocessor.

10.2.1.1 Using the Transmit command

To transmit data, one of the following sequences can be used:

1. All data to be transmitted to the label is written to the FIFO buffer while the Idle command is active. Then the command code for the Transmit command is written to the Command register.

   Remark: This is possible for transmission of a data stream up to 64 bytes.

2. The command code for the Transmit command is stored in the Command register. Since there is not any data available in the FIFO buffer, the command is only enabled but transmission is not activated. Data transmission starts when the first data byte is written to the FIFO buffer. To generate a continuous data stream on the RF interface, the microprocessor must write the subsequent data bytes into the FIFO buffer in time.

   Remark: This allows transmission of any data stream length but it requires data to be written to the FIFO buffer in time.

3. Part of the data transmitted to the label is written to the FIFO buffer while the Idle command is active. Then the command code for the Transmit command is written to the Command register. While the Transmit command is active, the microprocessor can send further data to the FIFO buffer. This is then appended by the transmitter to the transmitted data stream.

   Remark: This allows transmission of any data stream length but it requires data to be written to the FIFO buffer in time.

When the transmitter requests the next data byte to ensure the data stream on the RF interface is continuous and the FIFO buffer is empty, the Transmit command automatically terminates. This causes the internal state machine to change its state from transmit to idle.

When the data transmission to the label is finished, the TxIRq flag is set by the FSV9504 to indicate to the microprocessor transmission is complete.

Remark: If the microprocessor overwrites the transmit code in the Command register with another command, transmission stops immediately on the next clock cycle. This can produce output signals that are not in accordance with ISO/IEC 15693 or the ICODE1 protocol.

10.2.1.2 RF channel redundancy and framing

Each ISO/IEC 15693 transmitted frame consists of a Start Of Frame (SOF) pattern, followed by the data stream and is closed by an End Of Frame (EOF) pattern. All ICODE1 command frames comprise a start pulse followed by the data stream. The ICODE1 commands have a fixed length and do not require an EOF. These different phases of the transmission sequence can be monitored using the PrimaryStatus register ModemState[2:0] bits; see Section 10.2.4 on page 71.

Depending on the setting of the ChannelRedundancy register bit TxCRCEn, the CRC is calculated and appended to the data stream. The CRC is calculated according to the settings in the ChannelRedundancy register.

10.2.1.3 Transmission of frames with more than 64 bytes

To generate frames of more than 64 bytes, the microprocessor must write data to the FIFO buffer while the Transmit command is active. The state machine checks the FIFO buffer status when it starts transmitting the last bit of the data stream; the check time is marked in Figure 13 with arrows.

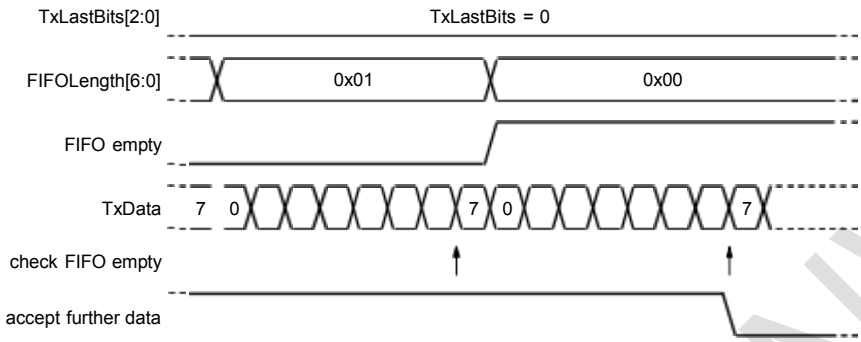


Fig 13. Timing for transmitting byte oriented frames

As long as the internal accept further data signal is logic 1, further data can be written to the FIFO buffer. The FSV9504 appends this data to the data stream transmitted using the RF interface.

If the internal accept further data signal is logic 0, the transmission terminates. All data written to the FIFO buffer after accept further data signal was set to logic 0 is not transmitted, however, it remains in the FIFO buffer.

10.2.2 Receive command 16h

Table 127. Receive command 16h

Command	Value	Action	Arguments and data	Returned data
Receive	16h	activates receiver circuitry	-	data stream

The Receive command activates the receiver circuitry. All data received from the RF interface is written to the FIFO buffer. The Receive command can be started either using the microprocessor or automatically during execution of the Transceive command.

Remark: This command can only be used for test purposes since there is no timing relationship to the Transmit command.

10.2.2.1 Using the Receive command

After starting the Receive command, the internal state machine decrements to the RxWait register value on every bit-clock. The analog receiver circuitry is prepared and activated from 3 down to 1. When the counter reaches 0, the receiver starts monitoring the incoming signal at the RF interface.

When the signal strength reaches a level higher than the RxThreshold register MinLevel[3:0] bits value, it starts decoding. The decoder stops when the signal can longer be detected on the receiver input pin RX. The decoder sets bit RxIRq indicating receive termination.

The different phases of the receive sequence are monitored using the PrimaryStatus register ModemState[2:0] bits; see Section 10.2.4 on page 71.

Remark: Since the counter values from 3 to 0 are needed to initialize the analog receiver circuitry, the minimum value for RxWait[7:0] is 3.

10.2.2.2 RF channel redundancy and framing

The ISO/IEC 15693 decoder expects the SOF pattern at the beginning of each data stream. When the SOF is detected, it activates the serial-to-parallel converter and gathers the incoming data bits. The ICODE1 decoder however, does not expect an SOF pattern at the start of each data stream, but activates the serial-to-parallel converter when the first data bit is received. Every completed byte is forwarded to the FIFO buffer.

If an EOF pattern is detected or the signal strength falls below the RxThreshold register MinLevel[3:0] bits setting, both the receiver and the decoder stop. Then the Idle command is entered and an appropriate response for the microprocessor is generated (interrupt request activated, status flags set).

When the ChannelRedundancy register bit RxCRCEn is set, a CRC block is expected. The CRC block can be one byte or two bytes depending on the ChannelRedundancy register CRC8 bit setting.

Remark: If the CRC block received is correct, it is not sent to the FIFO buffer. This is realized by shifting the incoming data bytes through an internal buffer of either one or two bytes (depending on the defined CRC). The CRC block remains in this internal buffer. Consequently, all data bytes in the FIFO buffer are delayed by one or two bytes. If the CRC fails, all received bytes are sent to the FIFO buffer including the faulty CRC.

10.2.2.3 Collision detection

If more than one label is within the RF field during the label selection phase, they both respond simultaneously. The FSV9504 supports the algorithm defined in ISO/IEC 15693 and the ICODE1 anti-collision algorithm to resolve label serial number data collisions by performing the anti-collision procedure. The basis for this procedure is the ability to detect bit-collisions.

Bit-collision detection is supported by the Manchester coding bit encoding scheme used in the FSV9504. If in the first and second half-bit of a subcarrier, modulation is detected, instead of forwarding a 1-bit or 0-bit, a bit-collision is indicated. The FSV9504 uses the RxThreshold register CollLevel[3:0] bits setting to distinguish between a 1-bit or 0-bit and a bit-collision. If the amplitude of the half-bit with smaller amplitude is larger than that defined by the CollLevel[3:0] bits, the FSV9504 flags a bit-collision using the error flag CollErr.

On a detected collision, the receiver continues receiving the incoming data stream. In the case of a bit-collision, the decoder sends logic 1 at the collision position.

Remark: As an exception, if bit ZeroAfterColl is set, all bits received after the first bit-collision are forced to zero, regardless whether a bit-collision or an unequivocal state has been detected. This feature makes it easier for the control software to perform the anti-collision procedure as defined in ISO/IEC 15693.

When the first bit collision in a frame is detected, the bit-collision position is stored in the CollPos register.

Table 128 shows the collision positions.

Table 128. Return values for bit-collision positions

Collision in bit	CollPos register value (Decimal)
SOF	0
Least Significant Bit (LSB) of the Least Significant Byte (LSByte)	1
…	…
Most Significant Bit (MSB) of the LSByte	8
LSB of second byte	9
…	…
MSB of second byte	16
LSB of third byte	17
…	…

If a collision is detected in the SOF, a frame error is flagged and no data is sent to the FIFO buffer. In this case, the receiver continues to monitor the incoming signal. It generates the correct notifications to the microprocessor when the end of the faulty input stream is detected. This helps the microprocessor to determine when it is next allowed to send data to the label.

10.2.2.4 Communication errors

The events which can set error flags are shown in Table 129.

Table 129. Communication error table

Cause	Flag bit
Received data did not start with the SOF pattern	FramingErr
CRC block is not equal to the expected value	CRCErr
Received data is shorter than the CRC block	CRCErr
A bit-collision is detected	CollErr

10.2.3 Transceive command 1Eh

Table 130. Transceive command 1Eh

Command	Value	Action	Arguments and data	Returned data
Transceive	1Eh	transmits data from FIFO buffer to the label and then automatically activates the receiver	data stream	data stream

The Transceive command first executes the Transmit command (see Section 10.2.1 on page 66) and then starts the Receive command (see Section 10.2.2 on page 68). All data transmitted is sent using the FIFO buffer and all data received is written to the FIFO buffer. The Transceive command can only be started by the microprocessor.

Remark: To adjust the timing relationship between transmitting and receiving, use the RxWait register. This register is used to define the time delay between the last bit transmitted and activation of the receiver. In addition, the BitPhase register determines the phase-shift between the transmitter and receiver clock.

10.2.4 States of the label communication

The status of the transmitter and receiver state machine can be read from bits ModemState[2:0] in the PrimaryStatus register.

The assignment of ModemState[2:0] to the internal action is shown in Table 131.

Table 131. Meaning of ModemState

ModemState [2:0]	State	Description
000	Idle	transmitter and/or receiver are not operating
001	TxSOF	transmitting the SOF pattern
010	TxData	transmitting data from the FIFO buffer (or redundancy CRC check bits)
011	TxEOF	transmitting the EOF pattern
100	GoToRx1	intermediate state passed, when receiver starts
	GoToRx2	intermediate state passed, when receiver finishes
101	PrepareRx	waiting until the RxWait register time period expires
110	AwaitingRx	receiver activated; waiting for an input signal on pin RX
111	Receiving	receiving data

10.2.5 Label communication state diagram

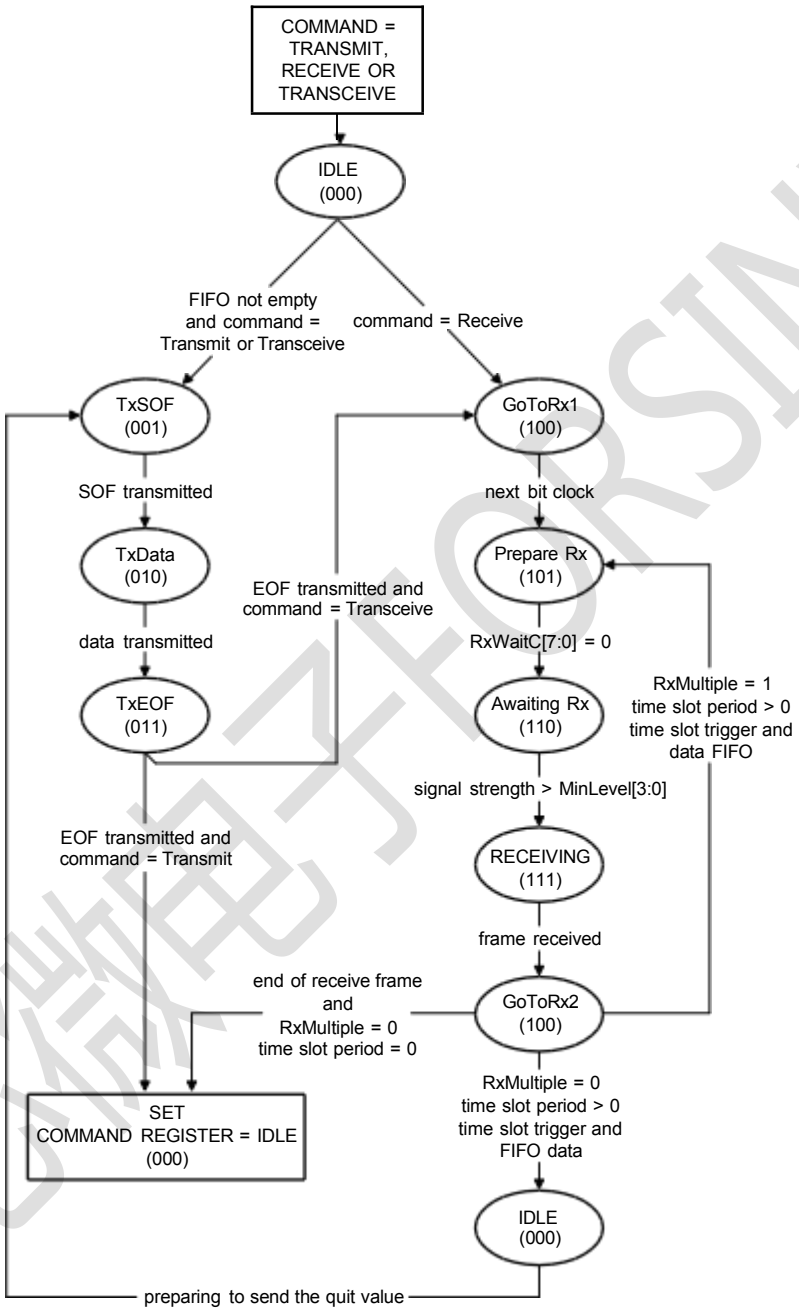


Fig 14. Label communication state diagram

10.3 EEPROM commands

10.3.1 WriteE2 command 01h

Table 132. WriteE2 command 01h

Command	Value	Action	FIFO	
			Arguments and data	Returned data
WriteE2	01h	get data from FIFO buffer and write it to the EEPROM	start address LSB	-
			start address MSB	-
			data byte stream	-

The WriteE2 command interprets the first two bytes in the FIFO buffer as the EEPROM start byte address. Any further bytes are interpreted as data bytes and are programmed into the EEPROM, starting from the given EEPROM start byte address. This command does not return any data.

The WriteE2 command can only be started by the microprocessor. It will not stop automatically but has to be stopped explicitly by the microprocessor by issuing the Idle command.

10.3.1.1 Programming process

One byte up to 16-byte can be programmed into the EEPROM during a single programming cycle. The time needed is approximately 5.8 ms.

The state machine copies all the prepared data bytes to the FIFO buffer and then to the EEPROM input buffer. The internal EEPROM input buffer is 16 bytes long which is equal to the block size of the EEPROM. A programming cycle is started if the last position of the EEPROM input buffer is written or if the last byte of the FIFO buffer has been read.

The E2Ready flag remains logic 0 when there are unprocessed bytes in the FIFO buffer or the EEPROM programming cycle is still in progress. When all the data from the FIFO buffer are programmed into the EEPROM, the E2Ready flag is set to logic 1. Together with the rising edge of E2Ready the TxIRq interrupt request flag shows logic 1. This can be used to generate an interrupt when programming of all data is finished.

Once E2Ready = logic 1, the WriteE2 command can be stopped by the microprocessor by sending the Idle command. Note that the WriteE2 command must not be stopped by starting another command before the E2Ready flag is set to logic 1, otherwise the content of the currently processed EEPROM block will either not be defined or the FSV9504 functionality may be irreversibly reduced.

Remark: During the EEPROM programming indicated by E2Ready = logic 0, the WriteE2 command cannot be stopped using any other command.

10.3.1.2 Timing diagram

Figure 15 shows programming five bytes into the EEPROM.

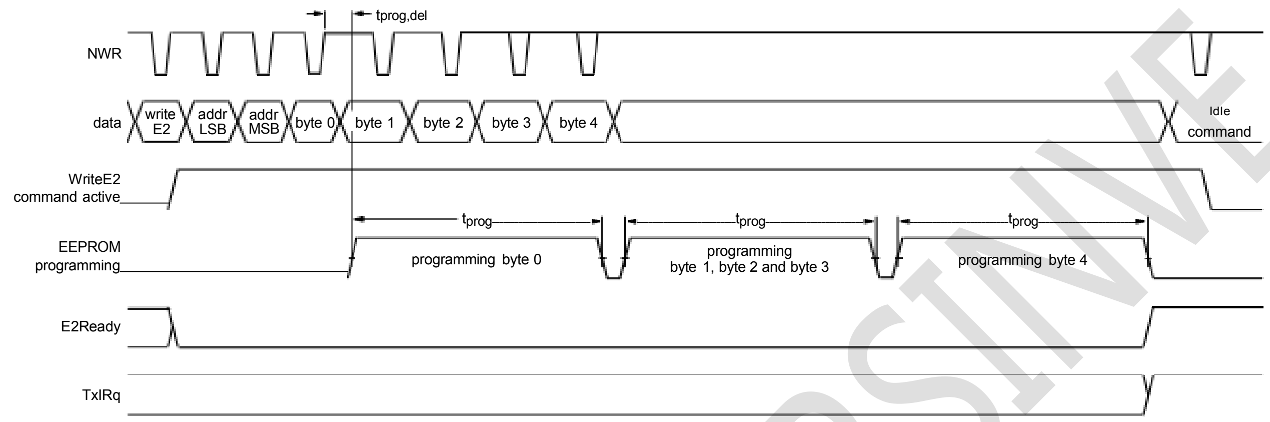


Fig 15. EEPROM programming timing diagram

Assuming that the FSV9504 finds and reads byte 0 before the microprocessor is able to write byte 1 ($t_{prog,del}$ = 300 ns). This causes the FSV9504 to start the programming cycle (t_{prog}), which takes approximately 2.9 ms to complete. In the meantime, the microprocessor stores byte 1 to byte 4 in the FIFO buffer.

If the EEPROM start byte address is 4Ch then byte 0 is stored at that address. The FSV9504 copies the subsequent data bytes into the EEPROM input buffer. Whilst copying byte 3, it detects that this data byte has to be programmed at the EEPROM byte address 4Fh. As this is the end of the memory block, the FSV9504 automatically starts a programming cycle.

Next, byte 4 is programmed at the EEPROM byte address 50h. As this is the last data byte, the E2Ready and TxIRq flags are set indicating the end of the EEPROM programming activity.

Although all data has been programmed into the EEPROM, the FSV9504 stays in the WriteE2 command. Writing more data to the FIFO buffer would lead to another EEPROM programming cycle continuing from EEPROM byte address 51h. The command is stopped using the Idle command.

10.3.1.3 WriteE2 command error flags

Programming is restricted for EEPROM block 0 (EEPROM byte address 00h to 0Fh). If you program these addresses, the AccessErr flag is set and a programming cycle is not started.

It is strictly recommended to use only the EEPROM address area indicated in the EEPROM memory organization given in Section 8.2 on page 9.

10.3.2 ReadE2 command 03h

Table 133. ReadE2 command 03h

Command	Value	Action	Arguments	Returned data
ReadE2	03h	reads EEPROM data and stores it in the FIFO buffer	start address LSB	data bytes
			start address MSB	
			number of data bytes	

The ReadE2 command interprets the first two bytes stored in the FIFO buffer as the EEPROM starting byte address. The next byte specifies the number of data bytes returned.

When all three argument bytes are available in the FIFO buffer, the specified number of data bytes is copied from the EEPROM into the FIFO buffer, starting from the given EEPROM starting byte address.

The ReadE2 command can only be triggered by the microprocessor and it automatically stops when all data has been copied.

Remark: It is strictly recommended to use only the EEPROM address area indicated in the EEPROM memory organization given in Section 8.2 on page 9.

10.4 Diverse commands

10.4.1 LoadConfig command 07h

Table 134. LoadConfig command 07h

Command	Value	Action	Arguments and data	Returned data
LoadConfig	07h	reads data from EEPROM and initializes the registers	start address LSB	-
			start address MSB	-

The LoadConfig command interprets the first two bytes found in the FIFO buffer as the EEPROM starting byte address. When the two argument bytes are available in the FIFO buffer, 32 bytes from the EEPROM are copied into the Control and other relevant registers, starting at the EEPROM starting byte address. The LoadConfig command can only be started by the microprocessor and it automatically stops when all relevant registers have been copied.

Remark: It is strictly recommended to use only the EEPROM address area indicated in the EEPROM memory organization given in Section 8.2 on page 9.

10.4.1.1 Register assignment

The 32 bytes of EEPROM content are written to the FSV9504 registers 10h to register 2Fh; see Section 8.2 on page 9 for the EEPROM memory organization.

Remark: The procedure for the register assignment is the same as it is for the StartUp initialization (see Section 8.7.3 on page 23). The difference is, the EEPROM starting byte address for the StartUp initialization is fixed to 10h (block 1, byte 0). However, it can be chosen with the LoadConfig command.

10.4.1.2 Relevant LoadConfig command error flags

Valid EEPROM starting byte addresses are between 10h and 60h.

10.4.2 CalcCRC command 12h

Table 135. CalcCRC command 12h

Command	Value	Action	Arguments and data	Returned data
CalcCRC	12h	activates the CRC coprocessor	data byte stream	-

The CalcCRC command takes all the data from the FIFO buffer as the input bytes for the CRC coprocessor. All data stored in the FIFO buffer before the command is started is processed.

This command does not return any data to the FIFO buffer but the content of the CRC can be read using the CRCResultLSB and CRCResultMSB registers.

The CalcCRC command can only be started by the microprocessor and it does not automatically stop. It must be stopped by the microprocessor sending the Idle command. If the FIFO buffer is empty, the CalcCRC command waits for further input before proceeding.

Remark: Do not use this command to calculate the quit value of ICODE1 tags because this terminates the Transceive command.

10.4.2.1 CRC coprocessor settings

Table 136 shows the parameters that can be configured for the CRC coprocessor.

Table 136. CRC coprocessor parameters

Parameter	Value	Bit	Register
CRC register length	8-bit or 16-bit CRC	CRC8	ChannelRedundancy
CRC algorithm	1 = algorithm using ISO/IEC 15693 or ISO/IEC 3309 0 = algorithm using ICODE1	CRC3309	ChannelRedundancy
Bit processing direction	shifts the MSB or LSB first into the CRC register	CRCMSBFirst	ChannelRedundancy
CRC preset value	any	CRCPresetLSB	CRCPresetLSB
		CRCPresetMSB	CRCPresetMSB

The CRC polynomial for the 8-bit CRC is fixed to $x^8 + x^4 + x^3 + x^2 + 1$.

The CRC polynomial for the 16-bit CRC is fixed to $x^{16} + x^{12} + x^5 + 1$.

10.4.2.2 CRC coprocessor status flags

The CRCReady status flag indicates that the CRC coprocessor has finished processing all the data bytes in the FIFO buffer. When the CRCReady flag is set to logic 1, an interrupt is requested which sets the TxIRq flag. This supports interrupt driven use of the CRC coprocessor.

When CRCReady and TxIRq flags are set to logic 1 the content of the CRCResultLSB and CRCResultMSB registers and the CRCErr flag are valid. The CRCResultLSB and CRCResultMSB registers hold the content of the CRC, the CRCErr flag indicates CRC validity for the processed data.

10.5 Error handling during command execution

If an error is detected during command execution, the PrimaryStatus register Err flag is set. The microprocessor can evaluate the status flags in the ErrorFlag register to get information about the cause of the error.

Table 137. ErrorFlag register error flags overview

Error flag	Related commands
AccessErr	WriteE2, ReadE2, LoadConfig
FIFOOvlf	no specific commands
CRCErr	Receive, Transceive, CalcCRC
FramingErr	Receive, Transceive
CollErr	Receive, Transceive

11. Limiting values

Table 138. Limiting values
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
T_{amb}	ambient temperature		−40	+150	°C
T_{stg}	storage temperature		−40	+150	°C
V_{DDD}	digital supply voltage		−0.5	+6	V
V_{DDA}	analog supply voltage		−0.5	+6	V
$V_{DD(TVDD)}$	TVDD supply voltage		−0.5	+6	V
V_i	input voltage (absolute value)	on any digital pin to DVSS	−0.5	V_{DDD} + 0.5	V
		on pin RX to AVSS	−0.5	V_{DDA} + 0.5	V

12. Characteristics

12.1 Operating conditions

Table 139. Operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb}	ambient temperature	-	−25	+25	+85	°C
V_{DDD}	digital supply voltage	DVSS = AVSS = TVSS = 0 V	4.5	5.0	5.5	V
V_{DDA}	analog supply voltage	DVSS = AVSS = TVSS = 0 V	4.5	5.0	5.5	V
$V_{DD(TVDD)}$	TVDD supply voltage	DVSS = AVSS = TVSS = 0 V	3.0	5.0	5.5	V
V_{ESD}	electrostatic discharge voltage	Human Body Model (HBM); 1.5 kΩ, 100 pF	-	-	1000	V
		Machine Model (MM); 0.75 µH, 200 pF	-	-	100	V

12.2 Current consumption

Table 140. Current consumption

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{DDD}	digital supply current	Idle command	-	8	11	mA
		Standby mode	-	3	5	mA
		Soft power-down mode	-	800	1000	µA
		Hard power-down mode	-	1	10	µA
I_{DDA}	analog supply current	Idle command; receiver on	-	25	40	mA
		Idle command; receiver off	-	12	15	mA
		Standby mode	-	10	13	mA
		Soft power-down mode	-	1	10	µA
		Hard power-down mode	-	1	10	µA
$I_{DD(TVDD)}$	TVDD supply current	continuous wave	-	-	150	mA
		pins TX1 and TX2 unconnected; TX1RFEn and TX2RFEn = logic 1	-	5.5	7	mA
		pins TX1 and TX2 unconnected; TX1RFEn and TX2RFEn = logic 0	-	65	130	µA

12.3 Pin characteristics

12.3.1 Input pin characteristics

Pins D0 to D7, A0, and A1 have TTL input characteristics and behave as defined in Table 141.

Table 141. Standard input pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{LI}	input leakage current		−1.0	-	+1.0	µA
V_{th}	threshold voltage	CMOS: V_{DDD} < 3.6 V	$0.35V_{DDD}$	-	$0.65V_{DDD}$	V
		TTL = 4.5 < V_{DDD}	0.8	-	2.0	V

The digital input pins NCS, NWR, NRD, ALE and A2 have Schmitt trigger characteristics, and behave as defined in Table 142.

Table 142. Schmitt trigger input pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{LI}	input leakage current		−1.0	-	+1.0	µA
V_{th}	threshold voltage	positive-going threshold; TTL = 4.5 < V_{DDD}	1.4	-	2.0	V
		CMOS = V_{DDD} < 3.6 V	$0.65V_{DDD}$	-	$0.75V_{DDD}$	V
		negative-going threshold; TTL = 4.5 < V_{DDD}	0.8	-	1.3	V
		CMOS = V_{DDD} < 3.6 V	$0.25V_{DDD}$	-	$0.4V_{DDD}$	V

Pin RSTPD has Schmitt trigger CMOS characteristics. In addition, it is internally filtered by a RC low-pass filter which causes a propagation delay on the reset signal.

Table 143. RSTPD input pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{LI}	input leakage current		−1.0	-	+1.0	µA
V_{th}	threshold voltage	positive-going threshold; CMOS = V_{DDD} < 3.6 V	$0.65V_{DDD}$	-	$0.75V_{DDD}$	V
		negative-going threshold; CMOS = V_{DDD} < 3.6 V	$0.25V_{DDD}$	-	$0.4V_{DDD}$	V
t_{PD}	propagation delay		-	-	20	µs

The analog input pin RX has the input capacitance and input voltage range shown in Table 144.

Table 144. RX input capacitance and input voltage range

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_i	input capacitance		-	-	15	pF
$V_{i(dyn)}$	dynamic input voltage	V_{DDA} = 5 V; T_{amb} = 25 °C	1.1	-	4.4	V

12.3.2 Digital output pin characteristics

Pins D0 to D7, SIGOUT and IRQ have TTL output characteristics and behave as defined in Table 145.

Table 145. Digital output pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OH}	HIGH-level output voltage	V_{DDD} = 5 V; I_{OH} = −1 mA	2.4	4.9	-	V
		V_{DDD} = 5 V; I_{OH} = −10 mA	2.4	4.2	-	V
V_{OL}	LOW-level output voltage	V_{DDD} = 5 V; I_{OL} = 1 mA	-	25	400	mV
		V_{DDD} = 5 V; I_{OL} = 10 mA	-	250	400	mV
I_O	output current	source or sink; V_{DDD} = 5 V	-	-	10	mA

Remark: Pin IRQ can be configured as open collector which causes the V_{OH} values to be no longer applicable.

12.3.3 Antenna driver output pin characteristics

The source conductance of the antenna driver pins TX1 and TX2 for driving the HIGH-level can be configured using the CwConductance register's GsCfgCW[5:0] bits, while their source conductance for driving the LOW-level is constant.

The antenna driver default configuration output characteristics are specified in Table 146.

Table 146. Antenna driver output pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OH}	HIGH-level output voltage	$V_{DD(TVDD)}$ = 5.0 V; I_{OL} = 20 mA	-	4.97	-	V
		$V_{DD(TVDD)}$ = 5.0 V; I_{OL} = 100 mA	-	4.85	-	V
V_{OL}	LOW-level output voltage	$V_{DD(TVDD)}$ = 5.0 V; I_{OL} = 20 mA	-	30	-	mV
		$V_{DD(TVDD)}$ = 5.0 V; I_{OL} = 100 mA	-	150	-	mV
I_O	output current	transmitter; continuous wave; peak-to-peak	-	-	200	mA

12.4 AC electrical characteristics

12.4.1 Separate read/write strobe bus timing

Table 147. Separate read/write strobe timing specification

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{LHLL}	ALE HIGH time		20	-	-	ns
t_{AVLL}	address valid to ALE LOW time		15	-	-	ns
t_{LLAX}	address hold after ALE LOW time		8	-	-	ns
t_{LLRWL}	ALE LOW to read/write LOW time	ALE LOW to NRD or NWR LOW	15	-	-	ns
t_{SLRWL}	chip select LOW to read/write LOW time	NCS LOW to NRD or NWR LOW	0	-	-	ns
t_{RWHSH}	read/write HIGH to chip select HIGH time	NRD or NWR HIGH to NCS HIGH	0	-	-	ns
t_{RLDV}	read LOW to data input valid time	NRD LOW to data valid	-	-	65	ns
t_{RHDZ}	read HIGH to data input high impedance time	NRD HIGH to data high-impedance	-	-	20	ns
t_{WLQV}	write LOW to data output valid time	NWR LOW to data valid	-	-	35	ns
t_{WHDX}	data output hold after write HIGH time	data hold time after NWR HIGH	8	-	-	ns
t_{RWLRWH}	read/write LOW time	NRD or NWR	65	-	-	ns
t_{AVRWL}	address valid to read/write LOW time	NRD or NWR LOW (set-up time)	30	-	-	ns
t_{WHAX}	address hold after write HIGH time	NWR HIGH (hold time)	8	-	-	ns
t_{RWHRWL}	read/write HIGH time		150	-	-	ns

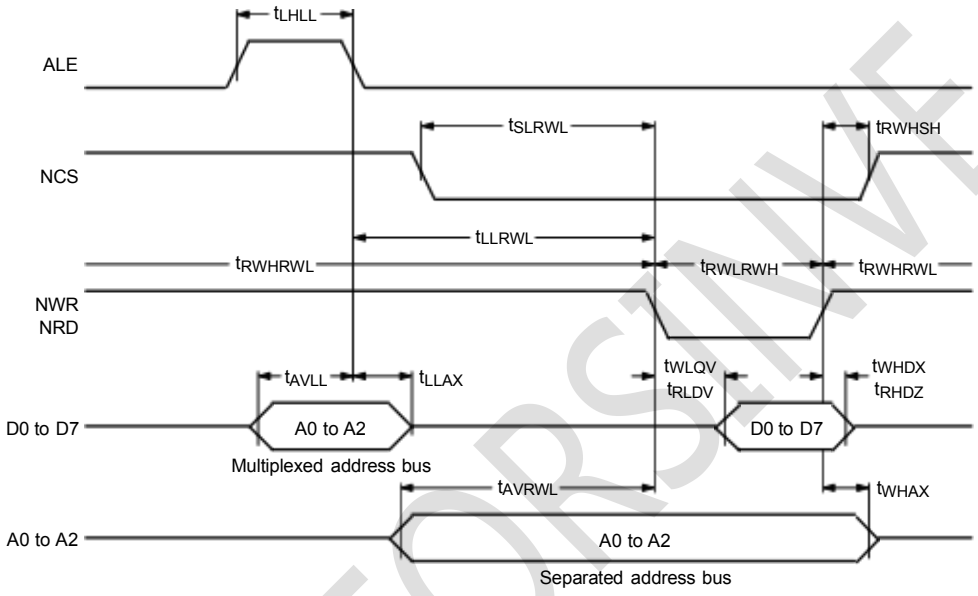


Fig 16. Separate read/write strobe timing diagram

Remark: The signal ALE is not relevant for separate address/data bus and the multiplexed addresses on the data bus do not care. The multiplexed address and data bus address lines (A0 to A2) must be connected as described in Section 8.1.3 on page 7.

12.4.2 Common read/write strobe bus timing

Table 148. Common read/write strobe timing specification

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{LHLL}	ALE HIGH time		20	-	-	ns
t_{AVLL}	address valid to ALE LOW time		15	-	-	ns
t_{LLAX}	address hold after ALE LOW time		8	-	-	ns
t_{LLDSL}	ALE LOW to data strobe LOW time		15	-	-	ns
t_{SLDSL}	chip select LOW to data strobe LOW time	NCS LOW to NDS LOW	0	-	-	ns
t_{DSHSH}	data strobe HIGH to chip select HIGH time		0	-	-	ns
t_{DSLDV}	data strobe LOW to data input valid time		-	-	65	ns
t_{DSHDZ}	data strobe HIGH to data input high impedance time		-	-	20	ns
t_{DSLQV}	data strobe LOW to data output valid time	NDS/NCS LOW	-	-	35	ns
t_{DSHQX}	data output hold after data strobe HIGH time	NDS HIGH (write cycle hold time)	8	-	-	ns
t_{DSHRWX}	RW hold after data strobe HIGH time	after NDS HIGH	8	-	-	ns
t_{DSLDSH}	data strobe LOW time		65	-	-	ns

Table 148. Common read/write strobe timing specification

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{AVDSL}	address valid to data strobe LOW time		30	-	-	ns
t_{RHAX}	address hold after read HIGH time		8	-	-	ns
t_{DSHDSL}	data strobe HIGH time	period between read/write sequences	150	-	-	ns
t_{WLDSL}	write LOW to data strobe LOW time	R/NW valid to NDS LOW	8	-	-	ns

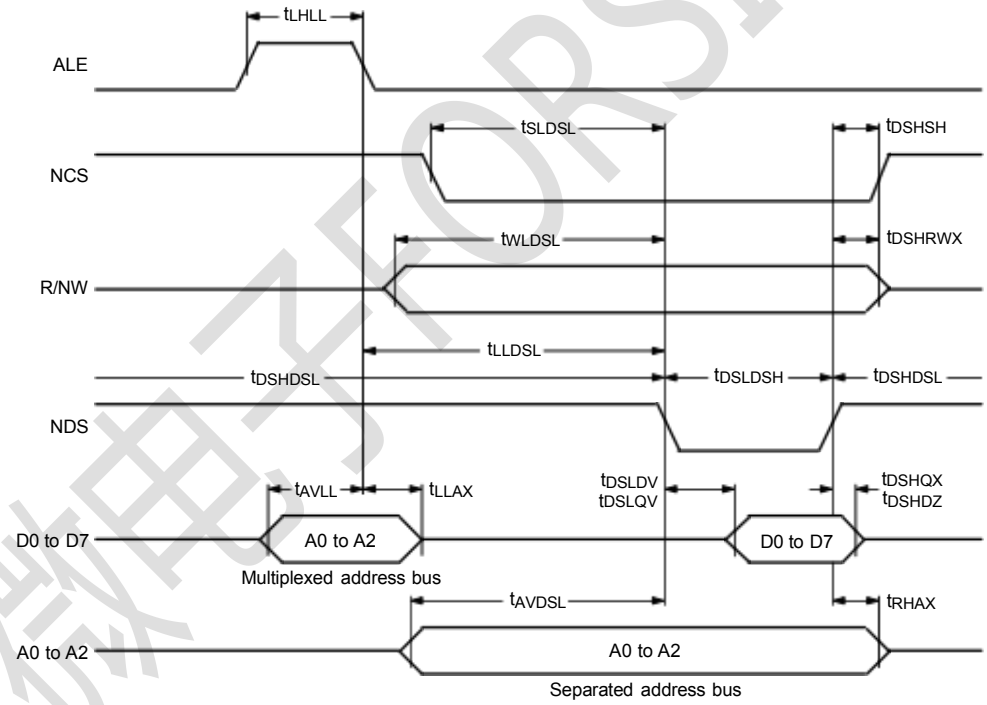


Fig 17. Common read/write strobe timing diagram

When separate address and data lines are used, the multiplexed addresses on the data bus do not use the ALE signal. When multiplexed address and data lines are used, the address lines (A0 to A2) must be connected as described in Section 8.1.3 on page 7.

12.4.3 EPP bus timing

Table 149. Common read/write strobe timing specification for EPP

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{ASLASH}	address strobe LOW time	nAStrb	20	-	-	ns
t_{AVASH}	address valid to address strobe HIGH time	multiplexed address bus set-up time	15	-	-	ns
t_{ASHAV}	address valid after address strobe HIGH time	multiplexed address bus hold time	8	-	-	ns

Table 149. Common read/write strobe timing specification for EPP

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{SLDSL}	chip select LOW to data strobe LOW time	NCS LOW to nDStrb LOW	0	-	-	ns
t_{DSHSH}	data strobe HIGH to chip select HIGH time	nDStrb HIGH to NCS HIGH	0	-	-	ns
t_{DSLDV}	data strobe LOW to data input valid time	read cycle	-	-	65	ns
t_{DSHDZ}	data strobe HIGH to data input high impedance time	read cycle	-	-	20	ns
t_{DSLQV}	data strobe LOW to data output valid time	nDStrb LOW	-	-	35	ns
t_{DSHQX}	data output hold after data strobe HIGH time	nDStrb HIGH	8	-	-	ns
t_{DSHWX}	write hold after data strobe HIGH time	nWrite	8	-	-	ns
t_{DSLDSH}	data strobe LOW time	nDStrb	65	-	-	ns
t_{WLDSL}	write LOW to data strobe LOW time	nWrite valid to nDStrb LOW	8	-	-	ns
$t_{DSL-WAITH}$	data strobe LOW to WAIT HIGH time	nDStrb LOW to nWait HIGH	-	-	75	ns
$t_{DSH-WAITL}$	data strobe HIGH to WAIT LOW time	nDStrb HIGH to nWait LOW	-	-	75	ns

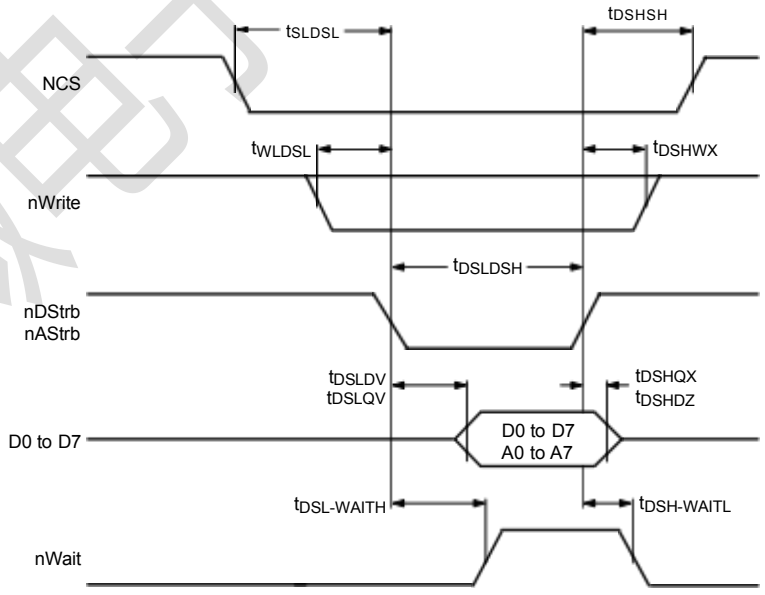


Fig 18. Timing diagram for common read/write strobe; EPP

Remark: Figure 18 does not distinguish between the address write cycle and a data write cycle. The timings for the address write and data write cycle are different. In EPP mode, the address lines (A0 to A2) must be connected as described in Section 8.1.3 on page 7.

12.4.4 Clock frequency

The clock input is pin OSCIN.

Table 150. Clock frequency

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{clk}	clock frequency	checked by the clock filter	-	13.56	-	MHz
δ_{clk}	clock duty cycle		40	50	60	%
t_{jit}	jitter time	of clock edges	-	-	10	ps

The clock applied to the FSV9504 acts as a time constant for the synchronous system's encoder and decoder. The stability of the clock frequency is an important factor for ensuring proper performance. To obtain highest performance, clock jitter must be as small as possible. This is best achieved using the internal oscillator buffer and the recommended circuitry; see Section 8.8 on page 24.

13. EEPROM characteristics

The EEPROM size is 8 × 16 × 8 = 1024 bit.

Table 151. EEPROM characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$N_{endu(W\_ER)}$	write or erase endurance	erase/write cycles	100000	-	-	Hz
t_{ret}	retention time	$T_{amb} \leq 55$ °C	10	-	-	year
t_{er}	erase time		-	-	2.9	ms
$t_{a(W)}$	write access time		-	-	2.9	ms

14. Application information

14.1 Typical application

14.1.1 Circuit diagram

Figure 19 shows a typical application where the antenna is directly matched to the FSV9504:

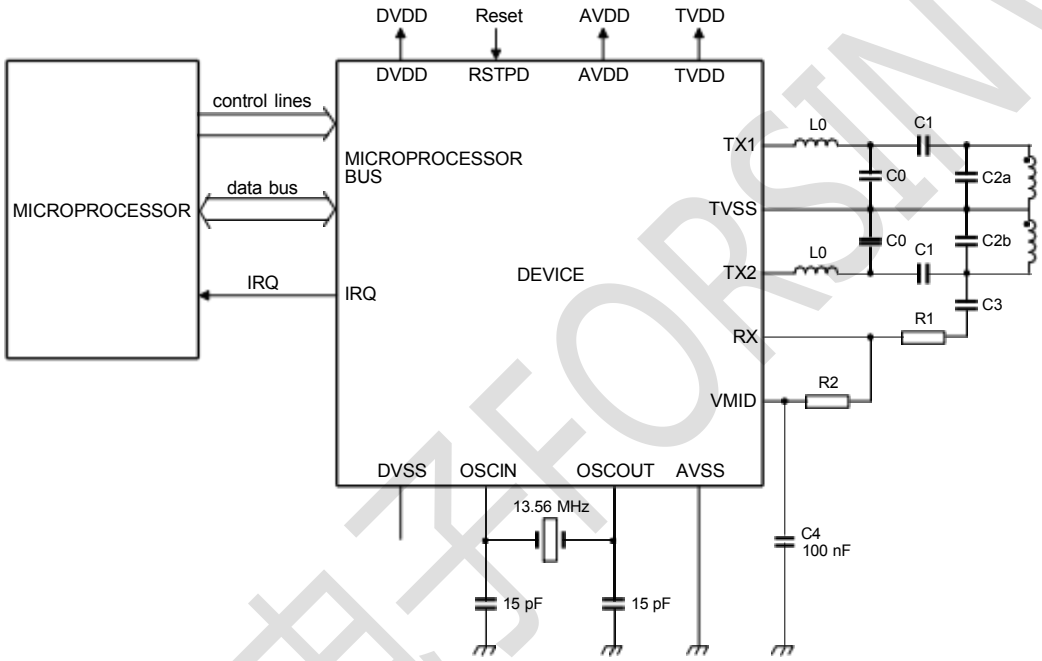


Fig 19. Application example circuit diagram: directly matched antenna

14.1.2 Circuit description

The matching circuit consists of an EMC low-pass filter (L0 and C0), matching circuitry (C1 and C2), a receiver circuit (R1, R2, C3 and C4) and the antenna itself.

Refer to the Application note Ref. 1 for more detailed information about designing and tuning an antenna.

14.1.2.1 EMC low-pass filter

The ICODE1 system operates at a frequency of 13.56 MHz. This frequency is generated by a quartz oscillator to clock the FSV9504. It is also the basis for driving the antenna using the 13.56 MHz carrier. This not only causes power emissions at 13.56 MHz, it also emits power at higher harmonics. International EMC regulations define the amplitude of the emitted power over a broad frequency range. To meet these regulations, appropriate filtering of the output signal is required.

A multilayer board is recommended to implement a low-pass filter as shown in Figure 19. The low-pass filter consists of the components L0 and C0. The recommended values are given in Application note Ref. 1.

Remark: To achieve best performance, all components must be at least equal in quality to those recommended.

Remark: The layout has a major influence on the overall performance of the filter.

14.1.2.2 Antenna matching

Due to the impedance transformation of the low-pass filter, the antenna coil has to be matched to a given impedance. The matching elements C1 and C2 can be estimated and have to be fine tuned depending on the design of the antenna coil.

The correct impedance matching is important to ensure optimum performance. The overall quality factor has to be considered to guarantee a proper ICODE1 communication scheme. Environmental influences have to considered and common EMC design rules.

Refer to Application note Ref. 1 for details.

Remark: Do not exceed the current limits ($I_{DD(TVDD)}$), otherwise the chip might be destroyed.

Remark: The overall 13.56 MHz RFID proximity antenna design in combination with the FSV9504 IC does not require any specialist RF knowledge. However, all relevant parameters have to be considered to guarantee optimum performance and international EMC compliance.

14.1.2.3 Receiver circuit

The internal receiver of the FSV9504 makes use of both subcarrier load modulation side-bands in the label response signal. No external filtering is required.

It is recommended to use the internally generated VMID potential as the input potential for pin RX. This VMID DC voltage level has to be coupled to pin RX using resistor (R2). To provide a stable DC reference voltage, a capacitor (C4) must be connected between VMID and ground.

The AC voltage divider of R1 + C3 and R2 has to be designed taking in to account the AC voltage limits on pin RX. Depending on the antenna coil design and the impedance, matching the voltage at the antenna coil will differ. Therefore the recommended way to design the receiver circuit is to use the given values for R1, R2, and C3; refer to Application note Ref. 1. The voltage on pin RX can be altered by varying R1 within the given limits.

Remark: R2 is AC connected to ground using C4.

14.1.2.4 Antenna coil

The precise calculation of the antenna coil's inductance is not practicable but the inductance can be estimated using Equation 10. When designing an antenna, it is recommended that its shape is either circular or rectangular.

$$L_1\ [nH] = 2 l_1\ [cm] \cdot \left(\ln\left(\frac{l_1}{D_1}\right) - K\right) N_1^{1.8}$$

- l_1 = length of one turn of the conductor loop
- D_1 = diameter of the wire or width of the PCB conductor, respectively

- K = antenna shape factor (K = 1.07 for circular antennas and K = 1.47 for square antennas)
- N_1 = number of turns
- ln = natural logarithm function

The values of the antenna inductance, resistance, and capacitance at 13.56 MHz depend on various parameters such as:

- antenna construction (type of PCB)
- thickness of conductor
- distance between the windings
- shielding layer
- metal or ferrite in the near environment

Therefore a measurement of these parameters under real life conditions or at least a rough measurement and a tuning procedure is highly recommended to guarantee a reasonable performance. Refer to Application note Ref. 1 for details.

14.2 Test signals

The FSV9504 allows different kinds of signal measurements. These measurements can be used to check the internally generated and received signals using the serial signal switch as described in Section 8.11 on page 31.

In addition, the FSV9504 enables users to select between:

- internal analog signals for measurement on pin AUX
- internal digital signals for observation on pin SIGOUT (based on register selections)

These measurements can be helpful during the design-in phase to optimize the receiver's behavior, or for test purposes.

14.2.1 Measurements using the serial signal switch

Using the serial signal switch on pin SIGOUT, data is observed that is sent to the label or received from the label. Table 152 gives an overview of the different signals available.

Table 152. Signal routed to pin SIGOUT

SignalToSIGOUT	SIGOUTSelect	Signal routed to pin SIGOUT
0	0	LOW
0	1	HIGH
0	2	envelope
0	3	transmit NRZ
0	4	Manchester with subcarrier
0	5	Manchester
0	6	reserved
0	7	reserved
1	X	digital test signal

14.2.2 Analog test signals

The analog test signals can be routed to pin AUX by selecting them using the TestAnaSelect register TestAnaOutSel[4:0] bits.

Table 153. Analog test signal selection

Value	Signal Name	Description
0	VMID	voltage at internal node VMID
1	Vbandgap	internal reference voltage generated by the bandgap
2	VRxFollI	output signal from the demodulator using the I-clock
3	VRxFollQ	output signal from the demodulator using the Q-clock
4	VRxAmpI	I-channel subcarrier signal amplified and filtered
5	VRxAmpQ	Q-channel subcarrier signal amplified and filtered
6	VCorrNI	output signal of N-channel correlator fed by the I-channel subcarrier signal
7	VCorrNQ	output signal of N-channel correlator fed by the Q-channel subcarrier signal
8	VCorrDI	output signal of D-channel correlator fed by the I-channel subcarrier signal
9	VCorrDQ	output signal of D-channel correlator fed by the Q-channel subcarrier signal
A	VEvalL	evaluation signal from the left half-bit
B	VEvalR	evaluation signal from the right half-bit
C	VTemp	temperature voltage derived from band gap
D	reserved	reserved for future use
E	reserved	reserved for future use
F	reserved	reserved for future use

14.2.3 Digital test signals

Digital test signals can be routed to pin SIGOUT by setting bit SignalToSIGOUT = logic 1. A digital test signal is selected using the TestDigiSelect register TestDigiSignalSel[6:0] bits. The signals selected by the TestDigiSignalSel[6:0] bits are shown in Table 154.

Table 154. Digital test signal selection

TestDigiSignalSel [6:0]	Signal name	Description
F4h	s_data	data received from the label
E4h	s_valid	when logic 1 is returned the s_data and s_coll signals are valid
D4h	s_coll	when logic 1 is returned a collision has been detected in the current bit
C4h	s_clock	internal serial clock: during transmission, this is the encoder clock during reception this is the receiver clock
D5h	rd_sync	internal synchronized read signal which is derived from the parallel microprocessor interface

Table 154. Digital test signal selection

TestDigiSignalSel [6:0]	Signal name	Description
C5h	wr_sync	internal synchronized write signal which is derived from the parallel microprocessor interface
96h	int_clock	internal 13.56 MHz clock
00h	no test signal	output as defined by the SIGOUTSelect register SIGOUTSelect[2:0] bits routed to pin SIGOUT

If test signals are not used, the TestDigiSelect register address value must be 00h.

Remark: All other values for TestDigiSignalSel[6:0] are for production test purposes only.

14.2.4 Examples of analog and digital test signals

Figure 20 shows the answer of an ICODE1 label IC to an unselected read command using the Q-clock receiving path. RX reference is given to show the Manchester modulated signal on pin RX.

The signal is demodulated and amplified in the receiver circuitry. Signal VRXAmpQ is the amplified side-band signal using the Q-clock for demodulation. The signals VCorrDQ and VCorrNQ were generated in the correlation circuitry. They are processed further in the evaluation and digitizer circuitry.

Signals VEvalR and VEvalL show the evaluation of the signal's right and left half-bit. Finally, the digital test signal s_data shows the received data. This is then sent to the internal digital circuit. A valid received data stream is indicated by signal s_valid.

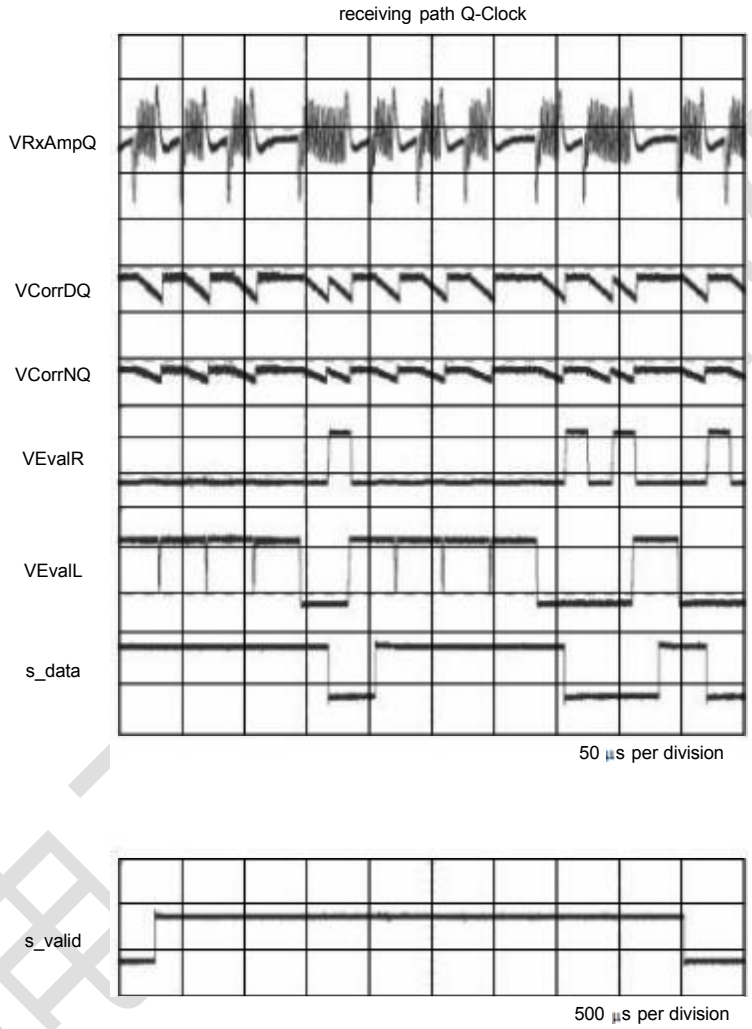
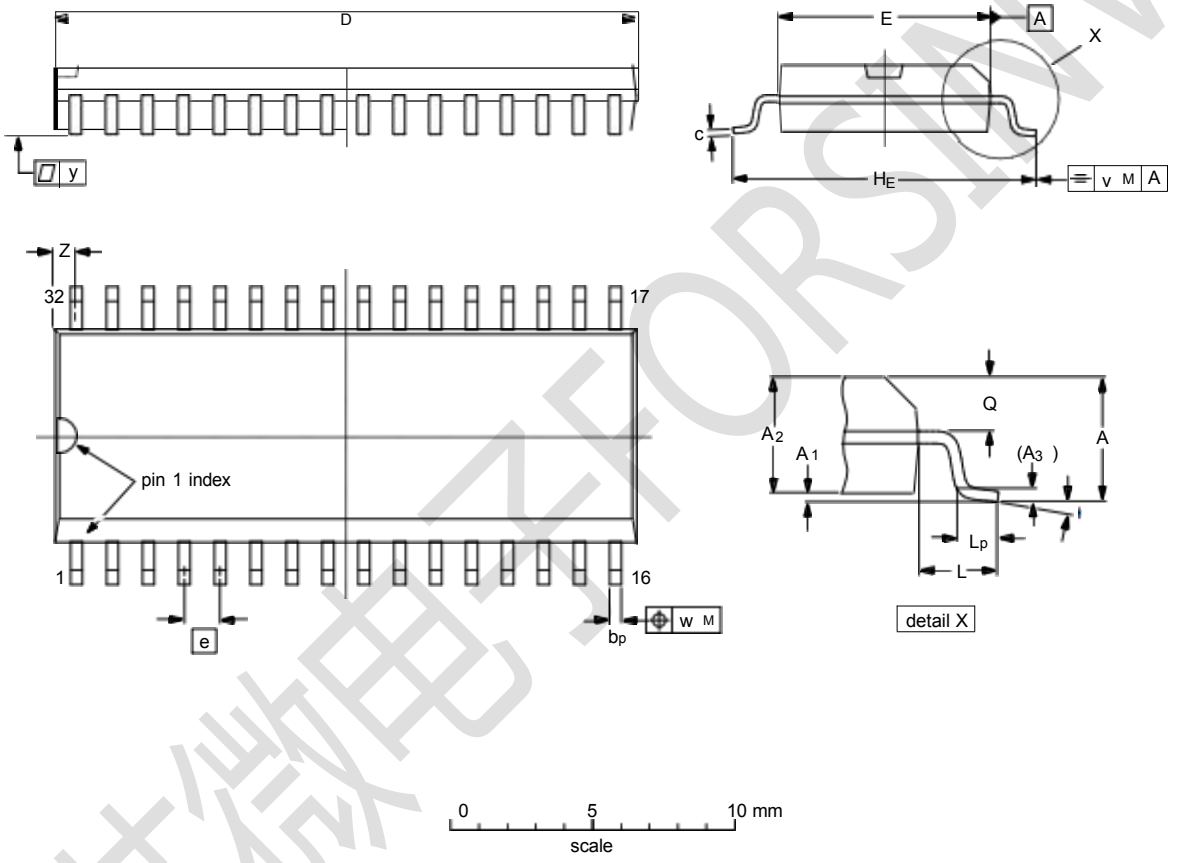


Fig 20. Q-clock receiving path

15. Package outline

SO32: plastic small outline package; 32 leads; body width 7.5 mm **SOT287-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.27 0.18	20.7 20.3	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.2 1.0	0.25	0.25	0.1	0.95 0.55	8^{o} 0^{o}
inches	0.1	0.012 0.004	0.096 0.089	0.01	0.02 0.01	0.011 0.007	0.81 0.80	0.30 0.29	0.05	0.419 0.394	0.055	0.043 0.016	0.047 0.039	0.01	0.01	0.004	0.037 0.022	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT287-1		MO-119				~~00-08-17~~ 03-02-19

Fig 21. Package outline SOT287-1

16. Abbreviations

Table 155. Abbreviations and acronyms

Acronym	Description
ASK	Amplitude-Shift Keying
BPSK	Binary Phase-Shift Keying
CMOS	Complementary Metal-Oxide Semiconductor
CRC	Cyclic Redundancy Check
EOF	End Of Frame
EPP	Enhanced Parallel Port
ETU	Elementary Time Unit
FIFO	First In, First Out
HBM	Human Body Model
IRQ	Interrupt ReQuest
LSB	Least Significant Bit
MM	Machine Model
MSB	Most Significant Bit
NRZ	None Return to Zero
POR	Power-On Reset
PCD	Proximity Coupling Device
PICC	Proximity Integrated Circuit Card
RZ	Return to Zero
SOF	Start Of Frame
SPI	Serial Peripheral Interface
TTL	Transistor Transistor Logic

17. References

[1] **Application note —** *MIFARE and ICODE1 MICORE Reader IC Family; Directly Matched Antenna Design*, document number: 0779xx.1

18. Revision

Document ID	Release date	Data sheet status	Change notice	Supersedes
FSV9504				

21. Tables

22. Figures

23. Contents